BLE Demo Implementation

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# Overview

This document serves as the design output document. It contains details of implementation as well as design choices to match specifications.

TODO:

Check default state of enable signals with PU/PD resistors

### Classification and Standards

This design falls under IPC Class 1 based on the class definitions. Class 1 refers to general electronic products with a limited lifespan and is the most relaxed regarding quality requirements. Examples of this class include toys, remotes, coffee makers, portable speakers, and electronics that prioritize function over longevity or performance under harsh conditions. Class 2 is reserved for devices that require continued performance and an extended life cycle with few outages. Examples in this category include smartphones, laptops, microwaves, televisions, etc etc. Failure of these devices are not typically catastrophic. Class 3 is subject to the strictest of guidelines and is for mission-critical items, such as military radar or pacemakers.

Prior to selecting a via size, board density should be determined according to “The Best PCB Via Size Guidelines for your Design” by [Cadence](ia%20size).

IPC-2222 sets standard for minimum hole sizes.

# Hardware Design

## Board Stackup and Pours

Balancing copper. Application in 2-layer boards. Heat dissipation for power components.

Patch antennas look like ground pours.

Against

<https://www.youtube.com/watch?app=desktop&v=R3w4Go1s1hM&t=864s>

<https://electronics.stackexchange.com/questions/548556/4-layer-pcb-standard-stackup-grounding>

<https://smtnet.com/library/files/upload/Copper-Ground-Pours.pdf>

<https://www.allaboutcircuits.com/industry-articles/the-good-and-bad-of-grounded-copper-pour-the-emc-perspective/>

<https://www.ti.com/content/dam/videos/external-videos/ja-jp/9/3816841626001/6307563213112.mp4/subassets/crosstalk-on-pcb-layouts-presentation-quiz.pdf> - it’s complicated, generally not great.

In favor of filling signal layers with reference signal from nearby plane

<https://resources.altium.com/p/shaky-ground-arguments-against-copper-pours>

## STM32 Architecture and related toolchains

### STM32WB / STM32WBA / STM32WB0

The STM32WB line supports multiple wireless protocols. It does not support WiFi though, so Wifi is not available unless another chip is added. The B0 line is the simpler line of the three, the BA lime is the most robust.

The chips run for about $6 to $9 on Digikey. There are a few around $4-5 on Mouser.

STM32WB30CEU5A is a decent option to design with given available peripherals. WiFi and TCP Client with SSL is NOT available on this device, there is no stack for it.

Pin count estimation is given as follows:

* SPI – Serial Memory, 4
* SPI – MicroSD, 1
* JTAG – 4/5
* USB – 2
* Piezobuzzer – 1
* UART – Console, 4
* Character Display – 7 or 11
* LEDS – 2-3

STM32WB35CCU6A is a good option that offers FS USB (2.0) and 30 GPIO.

[Link to Mouser](https://www.mouser.com/ProductDetail/STMicroelectronics/STM32WB30CEU5A?qs=DPoM0jnrROXA98TRXR4iRg%3D%3D).

[Link to Datasheet](https://www.mouser.com/datasheet/2/389/dm00627896-1799525.pdf).

[STM32WB55RCV6](https://www.mouser.com/ProductDetail/STMicroelectronics/STM32WB55RCV6?qs=vLWxofP3U2y%2F21YKkPUpfQ%3D%3D) is a good option for USB and 49 I/O.

## RF Hardware Design Considerations

The device datasheet notes to refer to [AN5165](https://www.st.com/resource/en/application_note/an5165-how-to-develop-rf-hardware-using-stm32wb-microcontrollers-stmicroelectronics.pdf) “Development of RF hardware using STM32WB microcontrollers”. It notes that special care should be given for the layout of an RF board compared to a conventional circuit.

It is important to impedance match from both from the 1) antenna to the input of the chip and 2) chip output to the antenna. Poor matching introduces *lower sensitivity* and *lower signal amplitude* of the transmit signal. Maximum power is transferred when the internal resistance of the source (e.g. STM32) equals the resistance of the load (e.g. antenna). For a frequency-dependent signal, the load impedance must be the complex conjugate of the source impedance. Recall the complex conjugate has the same real part and an imaginary part with the same magnitude but opposite sign.

It is recommended to fill unused area on the top RF layer with a ground plane and connect that to the underlying ground layer (e.g. layer 2) and connect them with vias at 1/10th the wavelength of the RF signal.

## RF Design

The RF element of this design is driven by the internal front-end in the STM32WB. It is based on a direct modulation of the carrier in Tx and uses a low IF ([intermediate frequency](https://www.allaboutcircuits.com/textbook/radio-frequency-analysis-design/selected-topics/the-benefits-of-an-intermediate-frequency-in-rf-systems/#:~:text=Summary,known%20as%20a%20heterodyne%20receiver.)) architecture in Rx mode. Recall that the [baseband frequency](https://en.wikipedia.org/wiki/Baseband) is a frequency that has not been modulated to higher frequencies, the output of a microphone for example. The carrier frequency is typically the higher frequency signal that carries the information in a modulated form, 2.45 Ghz in the case of BLE and WiFi. An intermediate frequency is somewhere between the baseband and carrier frequencies. The benefits of IF are more relevant for RX receivers. It is noted that a benefit of IF receivers is that they allow the design to be optimized for one frequency because it first shifts down the received spectrum down to a band centered on the intermediate frequency. A lower frequency in practice also is kinder on circuit elements such as transistors and passive components, which deviate from their low frequency models. Transmission line effects also have more of an effect.

The AN5156 app note recommends to use a Pi matching network and a low-pass filter, they use the [DLF162500LT-5028A1](https://www.digikey.com/en/products/detail/tdk-corporation/DLF162500LT-5028A1/4321991).

It is common, and recommended, to use 0402 sized passive components to avoid parasitic inductances.

The STM32WB has the ability to provide higher output via the external power amplifier (PA) pin.

### Stackup and Trace Construction

Resource is [AN5165](https://www.st.com/resource/en/application_note/an5165-how-to-develop-rf-hardware-using-stm32wb-microcontrollers-stmicroelectronics.pdf).

Transmission lines can be implemented on external layers using microstrips and coplanar waveguides or in buried internal layers with striplines.

The typical material used in RF design is FR-4. STM indicates that 2 layer PCBs can be used but they must be limited to 0.8 to 1.0 mm to make 50 ohm lines. While this would pose an interesting design challenge to tackle, it is most likely adding unnecessary complexity for a first-pass designing with RF features. It is generally recommended that 4 layers be the minimum to have ample room to route as well as have full ground planes for RF coupling.

The default stackup from Osh Park looks to have a standard 0.2mm thickness for the prepreg layers with a core thickness of 0.9906mm.

Since the gap between the center trace and the nearby ground planes will be less than the width of the center trace, gap is first set at 6 mils to align with manufacturer limits (e.g. Osh Park has a limit A screenshot of a computer

AI-generated content may be incorrect.of 5 mil). This yields that trace width should be around 13.85 according to KiCad’s transmission line calculator. This is in the ballpark of the expected value, which is around 13 mil for the center conductor. This Hackaday [article](https://hackaday.io/project/162998-the-rise-and-fall-of-pulses/log/168604-osh-park-4-layer-coplanar-waveguide) describes a project using Osh Park’s 4-layer stackup and calculations for configuring 50 ohm lines. Their recommended width based on initial calculation and measured results for a gap of 6 mils is 13.4 mils.

Figure 1: 50 ohm transmission line calculations

Param set:

Effective E, 2.52, Z0 = 50.01

Track width: 0.3302 mm, 13 mil

Gap: 0.073 mm, 2.87 mil

<https://www.protoexpress.com/blog/antenna-integration-rf-design-guidelines-for-5g-pcbs/>

<https://www.infineon.com/dgdl/Infineon-AN91445_Antenna_Design_and_RF_Layout_Guidelines-ApplicationNotes-v09_00-EN.pdf?fileId=8ac78c8c7cdc391c017d073e054f6227>

If using CPWG, you can widen the ground plane around the 0402 component pads to try to keep the 50 ohm impedance.

The ground on each side of the trace shall be greater than according to [edaboard.com post](https://www.edaboard.com/threads/gap-width-for-grounded-coplanar-waveguide-grounded-cpw.153771/).

For JLCPCB basic stack:

L1/L2 separation = 0.2104 mm (8.28 mil)

S=10, W = 14.85

S=8, W = 14.21

S=6, W = 13.1

It is noted by [Cypress](https://www.infineon.com/dgdl/Infineon-AN91445_Antenna_Design_and_RF_Layout_Guidelines-ApplicationNotes-v09_00-EN.pdf?fileId=8ac78c8c7cdc391c017d073e054f6227) (Infineon) in section 16.2 that the gap between grounds [and the center conductor] in the top layer is less than the height of the substrate, otherwise the topology is mostly microstrip. Also ensure that the ground pour is wider than the gap between the groups.

0402 component width is 0.5mm (19.685 mil).

7628 – microstrip: 15 mils

### Matching Network

The design should utilize a Pi-style matching network to match the output RF1 trace to 50 ohms.

### Antenna Design

There are a few methods to add an antenna to this design. These include 1) a PCB antenna, 2) chip antenna, and 3) external wired antenna. The original specifications recommend a PCB antenna, specifically the PIFA-type. These come in a different variety, with the primary antenna looking like an F and another variant called a MIFA (meandered) that winds the antenna length to save space. These are both relatively common in IoT applications. I have personally seen the MIFA antenna be used in small BLE modules, like the [ATWINC1500](https://www.microchip.com/en-us/product/atwinc1500) by Microchip. I have also utilized a BLE module that uses a chip antenna in a past project with no noticeable performance issues, though range was not tested. In short, either antenna is most likely suitable for the final application. An external antenna is most likely the most robust and flexible, offers the best performance, and costs the most.

A short comparison between PCB antenna and chip ceramics points out a few characteristics that determine what is most appropriate for a design. Chips are both more compact but also most costly, though cost is difficult to quantify across the low-high volume scale. This is due to the cost of the ceramic component, any matching components, and differences in PCB footprint for the PCB antenna. However, in the larger discussion of cost, the design and testing for PCB antenna boards can greatly increase cost through multiple iterations and time spent because each board variation needs to be tested and design requires simulation to be done.

It is noted in the article [“Six Hidden Costs in a Wireless SoC”](https://www.silabs.com/documents/public/white-papers/six-hidden-costs-in-a-wireless-soc-design.pdf) that application notes providing antenna designs for their RF circuits often do not guarantee sufficient results even when followed to the letter. There are too many factors, such as board or SMT component properties, that can vary from the original test setup to guarantee the measured performance.

Chip ceramics should be less susceptible to environmental changes as well and overall easier to use in a design. Since this is a project with a very limited scope, with potentially only 1-2 iterations, I reason that getting a PCB that “works well enough” to be able to program is most important. To properly tune an antenna requires additional tools and will be a time and financial investment. I will discuss potential ways to test my antenna shortly.

Cost aside, it seems that this project could benefit from a PCB antenna as the board is expected to be large enough to support a MIFA antenna and it is not for a wearable application. It is possible that once I test the first iteration of the board with the chip antenna that I design a 2nd version with a PCB antenna.

#### Ceramic Chip Antenna

Antennas can be compared using a few properties. The Voltage Standing Wave Ratio (VSWR) is a measure of how efficiently input power is transmit through the device to the output, specifically by calculating the ratio of the maximum to the minimum voltage . This ratio can also be derived from impedances. Typically, you want a lower ratio that is [around 2 or less](https://www.antenna-theory.com/definitions/vswr.php#:~:text=In%20general%2C%20if%20the%20VSWR%20is%20under%202%20the%20antenna%20match%20is%20considered%20very%20good%20and%20little%20would%20be%20gained%20by%20impedance%20matching.).

Another factor is antenna gain, typically given in dBi. It is the ratio between the gain of the antenna compared to that of an isotropic antenna, which radiates uniformly in all directions. Thus, a gain of 5 mean that the antenna will emit more power in a given direction compared to the isotropic antenna. Johanson Technology notes in their “Understanding Chip Antennas” [handbook](https://www.johansontechnology.com/docs/3763/antenna-handbook.pdf) that chip antenna gain ranges from -6 dBi to +1.0 dBi.

It is noted that a sufficiently large ground plane is important for

<https://www.johansontechnology.com/docs/3763/antenna-handbook.pdf>

TDK ANT016008LCS2442MA2

Best Johanson  
[**2450AT45A0100001E**](https://www.johansontechnology.com/docs/3919/Antenna-2450AT45A0100001E-Rev4.0.pdf)

**Best Abracon**

[AMCA72-2R470G-S1F-T4](https://www.mouser.com/ProductDetail/ABRACON/AMCA72-2R470G-S1F-T4?qs=AAveGqk956HomprAQPZhxg%3D%3D)

RF Switch:

https://www.murata.com/en-us/products/connector/switchconnector

**2450AT42A0100001E**

**AMCA31-2R450G-S1F-T3 – ABRACON,** [**PHIL’S LAB RECOMMENDED**](https://www.youtube.com/watch?v=UQBMROv7Dy4)

<https://www.ti.com/lit/an/swra117d/swra117d.pdf> - TI’s PCB antenna

[AN048](https://www.ti.com/lit/an/swra092b/swra092b.pdf?ts=1742054597891&ref_url=https%253A%252F%252Fwww.google.com%252F) Texas Instruments – TI chip antenna guide

NanoVNA

<https://www.silabs.com/documents/public/white-papers/six-hidden-costs-in-a-wireless-soc-design.pdf>

<https://www.johansontechnology.com/docs/3777/johanson-technology-chip-antenna-selection-guide_oh3MCwi.pdf>

## STM32 Minimum Configuration

### Power Supply

In general, most components of the STM32 should be sourced by 3.3V. Section 6.1.6 shows the recommended decoupling capacitor values for each of the power pins. In general, sizing was determined according to:

0603: 1 pF to 100 nF

1 uF - 4.7 uF: 0805

10 uF - 22 uF: 1206

>47 uF: 1210

### External Clock

The external clock must be a 32 MHz crystal oscillator or sine or square wave. I have used crystals from ECS before and the closest at 32 MHz would be the [ECS-320-8-33-RWY-TR](https://www.digikey.com/en/products/detail/ecs-inc/ECS-320-8-33-RWY-TR/9648894) and it is cost-effective at around $0.43/u. The crystal recommended by the datasheet is the EXS00A-CS06654 from NDK from the NX2016SA series, which has an 8 pF load capacitance. The ECS part also has an 8 pf load capacitance. Additional capacitors are included to tune the board capacitance to the load capacitance. This can be calculated using , where . If C1 = C2, then

The clock signal can be output on MCO to expose the master clock signal.

See application note [AN5042](https://www.st.com/resource/en/application_note/an5042-how-to-calibrate-the-hse-clock-for-rf-applications-on-stm32-wireless-mcus-stmicroelectronics.pdf) “Precise HSE frequency and startup time tuning for STM32 wireless MCUs” on specific information for the main clock for the STM32WB line. It is noted that HSE configuration is very important for correct RF operation. The HSETUNE register sets the added load capacitance, ranging from 12-16 pf.

The recommend crystal specifications by STM ([video source](https://www.youtube.com/watch?v=qNJR9vL1D0c)) are as follows:

|  |  |
| --- | --- |
| Parameter | Value |
| Load Capacitance | 8 pF |
| Frequency tolerance |  |
| Frequency vs temperature (ref. to +25C) |  |

[ECS-320-8-33B2-CTN-TR3](https://www.mouser.com/ProductDetail/ECS/ECS-320-8-33B2-CTN-TR3?qs=Jm2GQyTW%2Fbiv%2FbrQ%2F81iXQ%3D%3D)

### RTC Clock

The RTC clock is used to keep track of real-time and supplies the LSE clock. The OSC32\_IN and OSC32\_OUT ports connect directly to a crystal, resonator, or oscillator can be used to provide the signal.

The application note [AN2867](https://www.st.com/content/ccc/resource/technical/document/application_note/c6/eb/5e/11/e3/69/43/eb/CD00221665.pdf/files/CD00221665.pdf/jcr:content/translations/en.CD00221665.pdf) “Guidelines for oscillator design STM8AF/AL/S and STM32 MCUs/MPUs”

ECX-16

The crystal used by the reference design in AN5165 is the [MU00137-32.768K](https://www.digikey.com/en/products/detail/ndk-america-inc/MU00137-32-768K/9172005). Capacitors should be chosen using the same procedure that was used for the external clock.

### Unused Pins

AT0 and AT1 must be left floating, according to the datasheet. These are reserved for RF functions.

### STM32WB QSPI

Quad SPI can be mapped to different pins but in generally use:

QUADSPI\_BK1\_NCS – PB11 or PD3

QUADSPI\_ BK1\_CLK – PB10

QUADSPI\_ BK1\_IO0 – PB9 or PD4

QUADSPI\_ BK1\_IO1 – PB8 or PD5

QUADSPI\_ BK1\_IO2 – PD6

QUADSPI\_ BK1\_IO3 – PD7

Quad SPI for the STM32WB line has been documented by STM [here](https://www.st.com/resource/en/product_training/STM32WB-Memory-QuadSPI-interface-QUADSPI.pdf).

There are three modes. These include 1) indirect, 2) status-polling, 3) memory-mapped. Single data rate (SDR) and dual data rate (DDR) are supported. When the Cortex M4 frequency is below 50 MHz, the Quad-SPI block can use the same clock frequency for the bus. If higher, the prescaler must ensure a clock division of 2.

Indirect mode is when all operations are performed through registers, like classical SPI. Status-polling mode is when there is automatic periodical read of the flash memory status registers and interrupts are triggered when there is a match for certain conditions. Memory-mapped mode is when external flash memory is read like it is internal for read operations.

QSPI command contain up to 5 configurable phases. Each phase can be disabled/enabled, length adjusted, and a selectable number of lines. DMA support and interrupts flag can be used for data FIFO management.

### Reset Pin

The STM32 has a reset pin (NRST) that is used to reset the controller. It should be connected to JTAG connector for use in debugging and such. In addition to that, a small tactile switch (PTS526SK15SMTR2 LFS) has been added to provide a manual way to reset the controller. The switch provides a way to pull the NRST pin to ground, the reset state. A small capacitor is placed as close to the pin as possible for stability, per the datasheet. There is an internal pullup resistor to make the default state be the active state.

### ADC Input

### Boot Mode and Boot0

The STM32 can boot into the main application or into a bootloader mode. This is controlled by the state of the BOOT0 pin and the BOOT1 bit. The BOOT0 pin has an optional resistor pad to tie it to GND, making the default application the user-loaded code. A small switch is also included to allow for manual setting of the BOOT0 pin.

CJS-1200TA, pads under

[**CJS-1200TB1**](https://www.digikey.com/en/products/detail/nidec-components-corporation/CJS-1200TB1/2095031), pads out

[DS04-254-2-01BK-SMT-TR](https://www.mouser.com/ProductDetail/Same-Sky/DS04-254-2-01BK-SMT-TR?qs=wnTfsH77Xs4xXRFXKF0ssg%3D%3D)

[DS01-254-S-01BE](https://www.mouser.com/ProductDetail/Same-Sky/DS01-254-S-01BE?qs=wnTfsH77Xs7pnks1JfJqEQ%3D%3D) – both Mouser and Digikey

DS04-254-1L-01BK, both, raised

[DS04-254-2L-01BK](https://www.mouser.com/ProductDetail/Same-Sky/DS04-254-2L-01BK?qs=wnTfsH77Xs6BlrR2fIN60w%3D%3D), flat

## BLE and Inverted-F Antenna

The STM32 has an 32 MHz crystal, per the requirement.

## WiFi and TCP Client

Not supported in the BLE enabled STM32 chips. Thus, it is the decision of the designer to omit this feature from this board.

## DMA Utilization

DMA can be used to move data between two locations quickly without CPU involvement. Priority can be programmed to handle multiple requests across the configurable channels. DMA should be used to configure peripheral-to-memory, memory-to-peripheral, or peripheral-to-peripheral transfers. Transfer size should be flexible.

uC Notes:

Supports transfer size of 2^16. Allows access to flash memory, SRAM, APB, and AHB peripherals. There are 7 independently configurable channels.

## High-Capacity Non-Volatile Memory

The board was specified to utilize a surface mount memory controller but also have a MicroSD housing to allow the use of external memory chips.

### Serial Memory

NAND Flash offers high memory density for the lowest cost in general. Commonly available sizes include up to 512 MB. For this application, a chip in the 124 MB range would suffice.

<https://www.digikey.com/en/products/detail/winbond-electronics/W25N01GVZEIG/15181734>

<https://www.mouser.com/ProductDetail/Winbond/W25N01GVZEIG-TR?qs=qSfuJ%252Bfl%2Fd6niBi0Qz1MPg%3D%3D>

NOR Flash has a large range of products on Mouser and on Digikey. Common sizes range up to 1 Gbit / 125 megabytes. Micron Technology, Infineon, and Macronix are primary manufacturers of the technology. Like NAND, NOR is erased on blocks such as 4 kbyte. NOR flash is suggested to be more reliable over time and common for permanent storage (compared to SD-card like removeable memory). Costs seems to range around $10-20 for such larger capacity chips.

FRAM and MRAM are both better for endurance and size but are quite expensive. Would require specialized application to utilize benefits.

A sufficient memory chip for the design is the 16 MB NOR Flash chip, MX25L12833FM2I-10G, from Macronix. It is relatively low-cost at $1.25 and can utilize QSPI. The device ships with the Quad Enable bit set to 0 as default, which puts it in SPI mode and the QSPI pins are linked to other functions such as write protect, DNU, and reset. When in QSPI mode, the Hardware Protection Mode (HPM) and RESET feature are disabled (only in the 8-pin package). The QSPI mode can be entered by writing the “EQIO” command over the SIO0 line. This means that the QSPI bus will have to be compatible with SPI operation to initialize the memory.

A pull-up resistor is placed on the CS line to ensure the device is deselected upon startup conditions.

<https://www.st.com/resource/en/product_training/STM32WB-Memory-QuadSPI-interface-QUADSPI.pdf>

If there was space, I could have routed traces to have 50 ohms impedance.

Other Options:

MT29F2G01ABAGDWB-IT:G TR – 2gbit, SPI, not sure about QSPI, cheap

AT25SF321B-SSHB-B – 32 Mbit, SOIC, QSPI, $0.57, NOR FLASH

W25Q16JVSSIQ – $0.36, 16 mbit, QSPI, NOR,

AT25SF041B-SSHB-T – $0.39, 4 Mbit, QSPI, NOR

MX25L12833FM2I-10G – $1.25, 128 Mbit (16 MB), QSPI, NOR

MX25L25645GM2I-08G – $2.87, 256 Mbti (32 MB), QSPI, NOR

### microSD Card

There are different types of microSD cards, including:

1. SDSC (Standard Capacity)
   1. Max 2GB
   2. FAT16
   3. Typical max transfer speed of 12.5 MB/s
2. SDHC (High Capacity)
   1. Max 32GB
   2. FAT32
   3. Bus speeds of 12.5 MB/s to 25 MB/s typical, up to 3938 MB/s depending on bus interfaces
   4. Interfaces: UHS-I, UHS-II, UHS-III, SD-Express
3. SDXC (Extended Capacity)
   1. Max 2TB
   2. FAT32 or exFAT
   3. Bus speeds of 12.5 MB/s to 25 MB/s typical, up to 3938 MB/s depending on bus interfaces
   4. Interfaces: UHS-I, UHS-II, UHS-III, SD-Express

In general, SD cards have 9 pins and micro. A standard SD card can operate in 3 modes: 1) SPI, 2) one-bit SD, and 3) Four-bit SD. Cards historically have used 3.3V since their introduction in 2000. Recent additions to the protocol allow cards to use 1.8V levels but may require the controller to initialize the card using 3.3V logic.

MicroSD pinout is standardized, listed below:

|  |  |  |
| --- | --- | --- |
| Pin Number | SD Name | SPI Name |
| 1 | DAT2 | X |
| 2 | CD / DAT3 | CS |
| 3 | CMD | DI |
| 4 | VDD | VDD |
| 5 | CLK | SCLK |
| 6 | VSS | VSS |
| 7 | DAT0 | DO |
| 8 | DAT1 | X |

The mode cannot be switched while power is applied. In this case, the SPI interface is easier to implement. Note also that SD cards must be read/written to in sectors (512 bytes). QSPI is not applicable.

SD cards may or may not have wear leveling available, it depends on the manufacturer.

A filesystem library will be needed to format data to the FAT-formatted card.

ESD protection is generally recommended to protect the connected circuitry from any ESD events created by the SD card. The [article](https://www.ti.com/lit/sg/sszb130d/sszb130d.pdf?ts=1740453764443&ref_url=https%253A%252F%252Fwww.google.com%252F) “System-Level ESD Protection Guide” by Texas Instruments gives a brief overview of ESD terms, designs, and important considerations. Note that the working voltage (also known as reverse stand-off voltage) is the voltage at which the diode will begin to conduct significant current when off. Thus, the working voltage should be at the maximum working voltage of your device, an example being a working voltage of 3.4V for a 3.3V logic rail. The clamp voltage is where the ESD device limits the voltage on the rail while sinking excess current. For digital interfaces such as USB, HDMI, or an SD card, unidirectional ESD devices are ideal as they have better protection against negative voltages.

The ESD devices selected are ESD5Z3.3T1G (single channel) and PUSB3AB4Z (4-channel).

The [article](https://resources.altium.com/p/how-to-design-microsd-power-circuits-without-destabilizing-on-board-voltage-supply) “How to Design Stable Micro SD Card Power Circuits in PCB Layouts” by Altium recommends that a capacitance value of 45 uF or greater will do. It also states that a typical micro SD consumes up to 100 mA at 3.3V.

It is noted that people report that SD cards in SPI mode fail to release the output line, causing a bus collision with other target devices on the same SPI line. A common fix to this issue seems to be to always send a dummy byte after the main transmission or to have separate SPI buses for devices.

### EEPROM

An additional EEPROM is included on the board to store runtime settings and provide flexibility in terms of what/how data is stored. The design has an SOIC-8 footprint for an EEPROM memory chip. The schematic and layout is designed specifically for the CAT24C256 from Onsemi, which is a 256 kbit EEPROM. It uses I2C to communicate with the controller. Depending on the 3 address pins, the I2C address is set by . The write protect pin inhibits write operations when pulled high but does have a pull-down resistor, making the default state “writeable”. Other variants using the same pinout with lower cost and lower capacity can be used with no change in the design.

## Memory Encryption

To enable encryption on memory,

## JTAG

The STM32WB55 supports the serial wire JTAG debug port (SWJ-DP) that enables either a serial wire debug or JTAG prove to be connected to the target. Debug is performed using only 2 pins instead of the five required by the JTAG. The JTAG TMS and TCK pins are shared with SWDIO and SWCLK and a specific sequence on the TMS pin is used to switch between the two modes. Reference 3.28.1 in device datasheet.

The pins required for JTAG are typically:

1. TDI (Test Data In)

2. TDO (Test Data Out)

3. TCK (Test Clock)

4. TMS (Test Mode Select)

5. TRST (Test Reset) optional.

The STM32 uses the reduced pin count protocol of JTAG (EEE 1149.7) that only uses two pins, a TMSC (test serial data) and TSC (test clock) pin. This is also known as cJTAG, for compact JTAG. This allows a star topology instead of requiring devices to be connected in series.

The pins on the STM32 are indicated to be:

54: JTMS\_SWDIO

56: JTCK\_SWCLK

To interface with the JTAG interface, the programmer could use the ST-LINK/V2 by STM which also supports SWD. The ISOL version features increased isolation between the computer and PCB. It comes with a connector for the standard 20 pin JTAG interface. The ST-LINK V3 has a MIPI10, STDC14, and MIPI20 connector that sport a 1.27 mm pitch.

## Serial Wire Debug

## Programming using UARTx

The device can also be programmed using the onboard bootloader which receives the firmware image over UARTx or USB. The BOOT0 pin (5) and BOOT1 option bit are used to select one of the three boot options. BOOT1 is an option bit, which are essentially pre-configure bits that are set at programming time. These are automatically loaded after a power-on reset. Thus, in order for the bootloader to be activated the BOOT1 bit should be set and the pin BOOT0 can controlled with a switch.

## Debugging Output

The SWO pin can route printf style debug statements to a serial out pin. The printf function ultimately calls a “print character” function that writes the data to the selected output such as UART or SWO pin. SWO can be left floating if not used and most debuggers should still work as intended.

## Power Configuration

The power requirements of the system are primarily driven by the RF components of the board since they are most sensitive. The STM32 is designed for low-power applications running off coin-cell batteries, drawing up to 7.8 mA when the highest power level (+6 dBm). It has an onboard SMPS that can be optionally used given a high enough VDD. It is noted that the integrated LDOs that feed the system, including the RF and digital circuits, can be sourced either from the integrated SMPS or an external source. However, the other subsystems are fed directly from their source.

There are several elements in the STM32 that are powered:

VDD: feeds I/Os, SMPS, RF, internal clocks by 1.71 to 3.6 V.

VDDA: ADC/Comparators fed by 1.62 to 3.6 V.

VDDUSB: for USB transceivers fed by external 3.0 to 3.6 V.

VLCD: for the LCD controller fed by 2.5 to 3.6 V.

There are three embedded regulators that supply most of the digital and RF circuits, the three being the main regulator (MR), low-power regulator (LPR), and the RF regulator (RFR). The MR is used in the run and sleep modes as well as stop 0 mode, the LPR is used in a low-power run/sleep modes as well as stop 1 and stop 2 modes. It is used to power the SRAM2a in standby as well. The RFR supplies the RF analog part. All regulators are powered down in standy and shutdown modes and the outputs go to a high impedance mode.

By default, the microcontroller is in run mode, range 1, after turning on.

### USB-C Bus and PD Controller ✅

The main power bus comes from USB PD.

VBUS has an ESD protection diode, the TVS1800DRV, added for safety. It is [recommended](https://www.ti.com/lit/an/slvaf82b/slvaf82b.pdf?ts=1714998779059) by TI for a PD voltage of 15V.

This board will not support a native battery to the main supply as that is beyond the scope of the design. This is because a common USB-C application would utilize a rechargeable battery which powers the system and USB-C is used to recharge the battery during operation. Thus, the USB-C controller should support the “dead battery” mode, where the device can be powered up with a dead battery state.

The TPS25730 is a decent option with good documentation as well as features to utilize. It supports dead battery mode and uses a resistor divider to set the I2C address as well as voltage min, max, and current bounds. It also contains an integrated protection FET for VBUS. The TPS is powered by VBUS or VIN\_3V3, the latter being the typical supply. Upon registering the dead battery condition, VBUS is used and VIN\_3V3 remains disabled until cleared using I2C. Thus, VIN\_3V3 could be hooked up to receive power from a 3.3V bus when it is available.

Four pins (ADCINx) set the voltage and current capabilities of the PDO to be requested. It is also used to set the I2C address. Since the device will be operating in dead battery mode and it appears the config lines are sampled only upon boot, an 8 position DIP switch (4-1825059-2 from TE Connectviity) is included to select two primary settings. The configuration involves sampling the voltage over a divider so the switch will select which resistor is used in the lower leg of the divider. The evaluation module [guide](https://www.ti.com/lit/ug/slvucp4/slvucp4.pdf?ts=1741359241704&ref_url=https%253A%252F%252Fwww.ti.com%252Fproduct%252FTPS25730) shows a similar resistor divider configuration setup and lists 100k as the upper leg resistor with a selectable resistor as the lower leg, with values recorded and verified by their DIV value when comparing the decode and DIV values in Table 8-1 of the TPS25730 datasheet. The decode value of 7 does not need a pulldown resistor and cab be tired directly to LDO\_3V3, so if a decode value of 7 is needed then no pulldown resistor should be selected / populated.

|  |  |  |
| --- | --- | --- |
| Decoded Value | Resistor (ohm) | DIV Value |
| 0 | 1.0k | 0.0099 |
| 1 | 5.10k | 0.0485 |
| 2 | 12.1k | 0.1079 |
| 3 | 23.2k | 0.1883 |
| 4 | 43.2k | 0.3017 |
| 5 | 115k | 0.5349 |
| 6 | 412k | 0.8047 |
| 7 | 2M | 0.9524 |

In order for a PDO to be selected, it must fit within the bounds of the setpoints specified by the TPS25730. If a profile does not match, VBUS will remain at 5V and limited current can be drawn; 500 mA for USB 2 and 900 mA for USB 3. While 5V / 900 mA might be suitable power level for device operation, I assume 500 mA will not be with all features like BLE, audio, and character display. Thus, it is important that a PDO is selected. The following table describes the options selectable through the switch. Note that ADCIN3/4 are used together to define the current capability and are linked. With 4 total combinations, I will pick the two edge cases for low-current and high-current modes.

|  |  |  |
| --- | --- | --- |
| Name | Option A | Option B |
| Min Voltage (ADCIN1) | 0 | 5V | 1 | 9V |
| Max Voltage (ADCIN2) | 1 | 9V | 3 | 12V |
| Sink Current (ADCIN3/4) | IN3: 1 | 1Anom  IN4: 0 | 1.5Amax | IN3: 3 | 3Anom  IN4: 1 | 3Amax |

At a minimum, the VBUS should see 5V minus a small factor from the sense resistor. At 5A, the drop over the 25 mOhm resistor should be 0.125V. Thus, the VBUS should reasonably have at least 4.8V on the line at all times.

### DC-DC Output for USB PD regulation

As the voltage output from the USB PD port can be negotiated, and range from 5-20V, the system should be prepared to regulate the VBUS down to a level suitable for an LDO to feed the rest of the circuitry. This is due to the design feature that a higher input voltage may be negotiated so that other components or expansions can have access to a higher power, such as in the case where a motor is to be added to the board. This is accomplished through a DC-DC buck converter. The logic bus should not require high levels of current but does need to provide a stable output. Thus, a 3A rated buck regulator could be sufficient.

Since 3.3V is the main line, it should be stable going into the system. Since there are typically concerns with switching converters adding noise to the system, the design utilizes a LDO after the switching converter to remove noise. The chosen buck converter is the [MP2348](https://www.monolithicpower.com/en/mp2348.html?srsltid=AfmBOooL3iI7wVF1rxo_PiJ6kU1UF4-XdB7CvVGoOtTbpMCHjWyELhaH), a high efficiency simple package that can provide up to 4A with a switching frequency of 650 kHz. The datasheets shows higher efficiencies for a lower voltage inputs (e.g. 6.5V) and higher voltage outputs (e.g. 5V). The minimum input voltage is 4.2V.

TPS62933. The F version has continuous current mode in order to keep low ripple in all conditions. The O version operates out of the noise band. Max duty cycle of 98%. To achieve low frequency efficiency, base version uses CCM > DCM > PFM where frequency is adjusted

ALT: <https://www.ti.com/product/TPS62933O>

The O version is ok, the P version is just a power-good variant that uses PG to signal if the power is ready. Output voltage is set by the voltage divider and . The is set to 10kohm resistor, . Solving for the top resistor:

At 500 kHz

1.68 uH minimum for 5V input

3.6 uH minimum for 9V input

4.56 uH minimum for 15V input

4.92 uH minimum for 20V input

5.056 uH minimum for 22.8 input

5.1 uH minimum for 24V input

5.22 uH minimum for for 27.7V input

5.23 uH minimum for for 28V input

Choosing nearest value of 5.1 uH or 5.6 uH. The TVS1800 clamping diode should clamp the input voltage at 22.8V. This sets the new K value of 0.396. The maximum from the datasheet, the calculated peak current is calculated as follow:

The current is calculated from the equation:

It follows that the inductor should have a rating of 5.1 uH, have a saturation current of 10 A, and RMS current rating of 6.5A.

The recommended inductor for this design from TI’s workbench is 5.6 uH. Higher inductor values increase cost and DCR but generally reduce ripple current. Using an inductor

A similar product to the one recommend in the datasheet is 74439346056.

**78433290510**

SDR1307-5R6ML

Shielded Inductors

|  |  |  |  |
| --- | --- | --- | --- |
| Inductor P/N | Manufacturer | Cost | Description |
| SRP8540A-5R6M | Bourns | 0.53 | 5.6 uH, 30 mohm, 7.6A rms, 17A sat |
| [SRP1038AA-5R6M](https://www.mouser.com/ProductDetail/Bourns/SRP1038AA-5R6M?qs=CiayqK2gdcL4nvewsi77Ug%3D%3D) | Bourns | 0.68 | 5.6 uH, 22.8 mOhms, 8A rms, 14.1A sat |
| [SRP6060FA-5R6M](https://www.mouser.com/ProductDetail/Bourns/SRP6060FA-5R6M?qs=MLItCLRbWsxLUQxbwaGgMA%3D%3D) | Bourns | 1.64 | 5.6 uH, 15.8 mOhms, 7.5A rms, 10 sat |
| 74439346056 | Wurth Elektronik | 4.04 | 5.6 uH, 15 mOhms, 9.9A rms. 9.9A, 13.6A sat |
| [PA5432.562NLT](https://www.mouser.com/ProductDetail/Pulse-Electronics/PA5432.562NLT?qs=pUKx8fyJudACRr0COJ8pwg%3D%3D) | Pulse Electronics | 1.91 | 5.6 uH, 15.9 mOhms, 9. |
| [IHLP4040DZER5R6M01](https://www.mouser.com/ProductDetail/Vishay-Dale/IHLP4040DZER5R6M01?qs=UUKq9QDXQ0k7O9bH7nql%2Fg%3D%3D) | Vishay/Dale | 1.31 | 5.6 uH, 17.6 mOhms, 8.5A rms, 16.0A sat |
| EXL1V0606-5R6-R | Eaton |  |  |

Choosing [SRP6060FA-5R6M](https://www.mouser.com/ProductDetail/Bourns/SRP6060FA-5R6M?qs=MLItCLRbWsxLUQxbwaGgMA%3D%3D) as it fits the specs and has a smaller size with low DCR for a good average price of $1.64.

100 mA seems to be the crossing point for a lot of designs from light load to more

TPS56637 – option 2,

TPS54335-2A – option 3, ok but older with higher resistance MOSFETS, [MOUSER](https://www.mouser.com/ProductDetail/Texas-Instruments/TPS54336ADDA?qs=1CfNGUMoiQ9kh21wjoJyjQ%3D%3D)

TPS62933 – option 4, good efficiency across whole range, 2021

TPS563300 – [link](https://www.ti.com/lit/ds/symlink/tps563300.pdf?ts=1733695302679&ref_url=https%253A%252F%252Fwww.ti.com%252Fproduct%252FTPS563300), good max duty cycle, decent mosfet resistance, 500 kHz fixed frequency, good efficiency, $0.87

TPS51386RJNR – $0.78, above 90% efficiency across VIN ranges, VQFN package and better thermal dissipation, new chip, V\_EN limited to 6,m Ven limited to 55.5V

A screenshot of a computer

Description automatically generated

It is noted that for 5V output, VIN should at least be 6.5V. The initial target operation is to regulate from 5V down to around 3.8V. The expected duty cycle is around 76% (3.8/5), but could be as high as 80% (3.8/4.8). The datasheet indicates there is a minimum off time of 190 ns. The period for a 650 kHz signal is 1.54 us. To adhere to the minimum off time, the max duty cycle is thus . If Vin is 4.8V, the max output can be 4.2V. If Vin is 5.0V, the output can be at max 4.38V.

The LDO chosen is the [**LD39200PU33R**](https://www.digikey.com/en/products/detail/stmicroelectronics/LD39200PU33R/5131797), which can output 2A with a maximum of 0.25V droupout and a PSSR of around 40-50 at 500 kHz. It is also a very cost effective chip at around $1/unit. While it does limit the current supply further, its cost effectiveness and other performance qualities make it the desired choice for this design. With a max 0.25V dropout, a suitable input voltage should be or greater. This provides some headroom for the LDO and some room for the buck converter to scale down. A nominal selection for the LDO is 3.6V.

There is some concern that the buck converter will be operating near or above its practical max duty cycle based on the note the note about providing a 6.5V input for a 5V output, a duty cycle of 76%. If this ratio is to be followed, the output voltage of the buck should be lowered to 3.6V at least to account for an input voltage of 4.8V. This could be the best compromise in terms of buck output and LDO input without adding components. In the case this is not sufficiency for the buck, the intermediate bus could be lowered a bit more: the LDO has a typical dropout of 135 mV, so a buck output of 3.435V could be used.

Regarding power dissipation, the buck converter at 2A output should see a dissipation of around . This dissipated power leads to a junction temperature of . If a 0.5A load is drawn by the system, the heat rise should be around 11C. This is acceptable.

#### Notes about inductor and load currents

In fixed frequency mode and in the high-side switch on time, the SW pin voltage swings up to approximately and the inductor current increases with slope . Note that this does not depend on the output current. When the high-side switch is turned off and the LS switch is turned on, the inductor current discharges through the low-side switch with a slope of . Note again that the slope does not depend on the output current. When the output current is always above 0, the mode is CCM. Thus, a larger inductor will decrease the slopes of both phases.

When the load current, e.g. 300 mA, is lower than half of the peak-to-peak inductor current in CCM, the devices enter DCM. At an even lighter load, pulse frequency modification is used to maintain high-efficiency. When either the minimum high-side on time, or the minimum peak inductor current is reached, the switching frequency decreased to maintain regulation. It is noted that the current comparator in the TPS catches the peak inductor current only, the average load current entering PFM varies with the application and external LC filters. The high-side MOSFET is turned on in bursts to provide energy to the load. When zero current crossing is detected, the low-side MOSFET is turned off. The lowest selectable frequency possible is 200 kHz. The minimum switching frequency, presumably when in light current mode, is 30 kHz.

Under high load currents near the maximum, such as 2A or 3A, the switching frequency can be increased to 1 MHz or so to accommodate the load change and higher input voltages.

Under low load currents

#### Buck regulator component configuration

Current into the enable pin should be limited to prevent excess current above 40 uA from flowing into the diode. The datasheet indicates this can be done with a pullup resistor connected to Vin. The equation given is . At maximum, the input voltage is 20V. This solves to: .

Soft start is governed by

The mode of the buck converter can be controlled by the MODE pin. These include:

1. Forced PWM
2. PFM with ultrasonic mode under light-load conditions
3. PFM mode without ultrasonic mode

The output voltage is set by a voltage divider. The datasheet gives . It also states thar a small R2 leads to considerable quiescent current loss while a large R2 makes FB noise sensitive. The recommended value for R1 is 40.2 kOhm across most ranges, including the 3.3V range. Choosing R1 to be 40.2 kOhm allows R2 to be set for an output of 3.6V. is given to be 802 mV in the datasheet.

Feedback current should be limited to less than 50 nA.

Final selection: MP2348, MP2384C, MP2384

MP2348: 90% efficiency over whole range, 95% efficiency at 5V in. 55 C/W ambient as measured on 2-layer PCB, 64x48mm. Supply voltage 4.2 to 24V. $1.75 on Mouser. 650 kHz or less at light loads. Seems to have a bit more ripple, perhaps 12-15 mV of ripple at high current.

MP2384: very low ripple of maybe 8 mV at light loads.

<https://www.mouser.com/ProductDetail/Monolithic-Power-Systems-MPS/MP9943GQ-P?qs=493kPxzlxfIUN%2FwqEBzqKg%3D%3D>

<https://www.mouser.com/ProductDetail/Monolithic-Power-Systems-MPS/MP9473GL-P?qs=eL8B9ti3n5MiWqok8H7asw%3D%3D>

<https://www.mouser.com/ProductDetail/Monolithic-Power-Systems-MPS/MP2384CGG-P?qs=GedFDFLaBXFncJRO10qr2A%3D%3D> – LOOKS GOOD, super efficienct, but faster 700 kHz frequency

<https://www.monolithicpower.com/en/documentview/productdocument/index/version/2/document_type/Datasheet/lang/en/sku/MP4423GQ-Z> -

<https://www.monolithicpower.com/en/documentview/productdocument/index/version/2/document_type/Datasheet/lang/en/sku/MP2384GG-Z> - good across whole range, above 90%, is a variant of the MP2384C. IT is said [that](https://forum.monolithicpower.com/t/mp2384-vs-mp2384c/1805?_gl=1*19uinvu*_gcl_au*MTI1Mjc1NDYwLjE3MzMzNjgyNzg.*_ga*MjAzMDI2Nzc3My4xNzMzMzY4Mjc4*_ga_XNRPF6L9DD*MTczMzU3ODg1MS40LjEuMTczMzU3ODg5OS4xMi4wLjA.&_ga=2.71038672.1779404359.1733578851-2030267773.1733368278) the C version will have a better vout ripple due to FCCM, but a worse efficiency. There is no pulse skip mode at light loads in the base version so it will have worse ripple.

**MP2395 – ok, but not as good for lower output voltages**

MP2328

MP2349

**MP2348 – looks pretty good**

[MP2315S](https://www.mouser.com/ProductDetail/Monolithic-Power-Systems-MPS/MP2315SGJ-Z?qs=Zwj7mHVHPHQK3n9ExaDQiw%3D%3D) – on Mouser for 2.29, simple package but up to 3A, good power efficiency at lower input voltages, 500 kHz switching frequency, max dissipation is 1.25W, Max duty cycle is 95% for Vfb = 750 mV

LDO Selection

[**LD39200PU33R**](https://www.digikey.com/en/products/detail/stmicroelectronics/LD39200PU33R/5131797), 2A out with 0.25V dropout at $0.99, PSSR around 44 dbs at 500 kHz

[**RP108J331D-T1-FE**](https://www.digikey.com/en/products/detail/nisshinbo-micro-devices-inc/RP108J331D-T1-FE/10215597), 3A out with 0.56V dropout at $1.36,

BUCK/BOOST

MP4245 – $6.1

MP28167-B – 4.24

MP28167-N

<https://www.monolithicpower.com/en/documentview/productdocument/index/version/2/document_type/Datasheet/lang/en/sku/MP28167GQ-A>

#### TPS62933 Layout Notes

The datasheet for the TPS gives some layout notes. These are discussed on section 12 of the datasheet.

### 3.3V for logic and STM32

The STM32 needs a stable 3.3V reference for most peripherals. The internal SMPS can be used to feed the main and RF regulators but not the low power regulator, wakeup domain, LCD, or analog domain, or USB domain. Thus, a regulator is required to adjust the output from the USB port. A DC-DC buck boost converter is used to provide a fixed output such as 3.6-4V to the downstream. It is noted that the STM32 indicates it uses very low power to run, perhaps 20 mA or less, by looking at the Power Consumption Calculator (PCC) tool in the STM32Cube IDE.

The selected default backlight display, [C404A-FTW-LW63](https://focuslcds.com/product/c404a-ftw-lw63/), can use up to 120 mA for the backlight.

A mini speaker, such as the CMS-151103-088SP from Same Sky, is an 8 ohm speaker with input power of 0.7W. This should correspond to a current usage of

A piezo buzzer should only use maybe 5-10 mA.

An SD card could 30-100 mA.

#### Low current draw considerations

In cases where system current draw is low and the USB input is set to 5V, the utility of the DC-DC switching regulator is not as great as the case when higher voltages are input into the system. Note that efficiency for the DC-DC block becomes mostly constant starting around 0.02 mA for the base, type O, and type P models. A quick analysis in the 5V case indicates whether the design should include a mode to swap between the using VBUS directly or always going through the buck converter.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Current | LDO Power Dissipated | DC-DC Power Dissipated | LDO Temp Rise, C | DC-DC Temp Rise, C |
| 50 mA | 85 mW | 20 mW | 3.4 | 1.2 |
| 100 mA | 170 mW | 40 mW | 6.8 | 2.4 |
| 200 mA | 340 mW | 80 mW | 13.6 | 4.8 |

Section 9.3.2 of the TPS6293x datasheet indicates that there is a minimum peak inductor current, rated at . It is anticipated that most downstream circuitry will not draw nearly that much on average. It is said that when the load current is less than half of the peak-to-peak current, the device will operate in DCM.

[TPS2120](https://www.ti.com/lit/ds/symlink/tps2120.pdf?ts=1734040247940&ref_url=https%253A%252F%252Fwww.ti.com%252Fproduct%252FTPS2120)

### VBAT for RTC

When VDD is not present, VBAT operation is automatically activated. When the microcontroller is supplied only from VBAT, as it would be when USB-C is disconnected, external interrupts and RTC alarm/events do not exit it from VBAT operation. The VBAT pin should be connected to the battery. The valid voltage range is from . In section 6.3.2 of the datasheet it is recommended that VBAT fall within . Current consumption data is given for 1.8V, 2.4V, 3.0V, and 3.6V. A very common battery type is the CR2032, which is a 3V coin-cell battery. It is nominally 3.2mm thick and 20mm in diameter.

The BAT-HLD-001 from TE Connectivity provides a cost-effective and simple battery holder.

### Audio Power Regulation

The audio component of this design requires at least one additional rail. The design of the audio component is discussed later in this document but, to continue discussion of power configuration, the audio chain requires at least 1.8V for analog and digital core components. To provide more power to the speaker, an additional rail that ranges from 3.6 – 5V also could be beneficial and potential configurations will be discussed.

The 1.8V could be generated relatively easily from the 3.6V rail using an LDO. Since the 3.3V rail feeding the RF circuit is generated from an LDO, this could be acceptable. However, since the speaker rail would benefit from a higher voltage, it could make sense to have a 2nd DC-DC switching regulator that regulates the USB PD voltage to 5V. The 1.8V rail could then be generated from this 2nd rail.

For the 1.8V rail, the [LDL112PV18R](https://www.mouser.com/ProductDetail/STMicroelectronics/LDL112PV18R?qs=Ok1pvOkw6%2FrJNgvWv3vE3g%3D%3D) LDO can output 1.8V from an input range of 1.6 to 5.5V with a max current of 1A. It has a low dropout voltage of 200 mV.

The 5V rail could be generated using a buck-boost converter or simply a buck converter with 100% duty cycle to allow for the default case of 5V coming from the USB. Since buck-boost converters are generally more costly compared to buck converters and it is not a strict requirement that an precise 5V rail be generated, as only the speaker power will see the 5V directly, a buck converter will be used.

The construction of the 5V rail must consider the 5V, 9V, 15V, and 20V cases. As long as the buck converter is rated for the higher voltages, generally there should not be any problems designing around the parameters. As the speaker may be off, light load efficiency is important. The ripple factor also will presumably be a significant factor, as audio reference levels should be noiseless and stable. The 5V input case could pose some issues with a dropout voltage attributed to the maximum duty cycle supported by a buck converter.

Most buck converters are limited by their maximum duty cycle relating to their architecture. In general, there needs to be switching to make sure the bootstrap capacitor remains charged. This ultimately limits the maximum duty cycle, limiting the upper limit of the output voltage given a certain input voltage. While some devices can support up to a 98% duty cycle, like the TPS62933 used for the 3.6V rail generation, this would cause a rail. While this is pretty close to 5V and acceptable given that it should only effect the maximum speaker output, I want to utilize a buck converter that supports 100% duty cycle, otherwise known as low dropout mode (LDO mode) by some manufacturers.

One option is the AP63300 (or AP63301), which supports LDO mode, has an efficiency of around 90% for 5V output with 12V input. The AP63301 does not have great light load efficiency because it operates in PWM mode but does sport a better ripple output. Both devices have a fixed switching frequency of 500 kHz.

The AP6330x has an undervoltage lockout voltage of 3.06V and disables the output if the input falls below that. It also has overvoltage protection, overcurrent protection, and thermal shutdown features.

The output voltage is set using a voltage divider, governed by the relationship . Diodes Incorporated provides recommended values for common outputs. For 5V output, and . Additionally, an inductor of 6.8 uH is recommended. and capacitors, , and .

The equation given to determine inductor value is . If using the 9V profile and keeping the inductor ripple current smaller by setting it to be 30% of the maximum load current, 3A, this yields that . The datasheet notes that an inductor in the 2.2 uH to 10 uH range with a DC current rating at least 35% higher than the max load current should be selected. The DC resistance should be minimized, ideally less than . A larger inductor improves efficiency under lighter loads, though this typically means internal resistance increases which leads to increase power loss. The inductor’s saturation current rating should be selected according to the peak current, calculated using . For load current of 3A, . If there is a set 1A max current, .

### EXTRA NOTES

Buck converters: Low dropout mode (LDO mode)

TPS54231 – has LDO mode, 90% efficiency with Vin = 5

TPS54302

TPS62135RGXR – 100% but limited to 17V so we would lose the 20V profile, 80% efficient for most of range.

MP8715 – 100%, good input range, fixed frequency, expensive at $4

AP63300 -

Buck Boost converters: Starting around $3.83, Monolithic Power Systems is cheaper, in contrast my chosen buck is $1.

TPS55289

TPS55287

In general, analog and digital power rails should be isolated if possible.

Ferrite beads to isolate main line? There are different types of ferrite beads, one being a power inductor that is designed to have low loss. The main application to use a ferrite bead is for when you have a low-current device sensitive to noise, such as an analog component, and it is powered through a DC-DC switching regulator ([reference](https://youtu.be/HaLMjVkKYMw?si=lBo_Nns5E9gPTPik&t=1213)). At minimum, the ferrite filter pole has to be an order of magnitude lower than the frequency generating noise. An alternative to a ferrite filter is using an LDO.

[LDL1117S18R](https://www.mouser.com/ProductDetail/STMicroelectronics/LDL1117S18R?qs=AQlKX63v8RuvMlpR0ZSWFQ%3D%3D)

[LDL112PV18R](https://www.mouser.com/ProductDetail/STMicroelectronics/LDL112PV18R?qs=Ok1pvOkw6%2FrJNgvWv3vE3g%3D%3D), good package and still cheap

[LD49100PU18RY](https://www.mouser.com/ProductDetail/STMicroelectronics/LD49100PU18RY?qs=DPoM0jnrROWE8S4gij7e0w%3D%3D)

## Multiple Power Sources

The design should have at least 2 power sources, the main bus and a local battery for RTC operations. An additional battery source or input terminal, besides USB-C, can be included for convenience or evaluation.

### Local Battery

Typically batteries for battery supplies operate at 3V, the CR2023 being one example. These are typically 20mm in diameter.

[TE Con Battery Holder Link](https://www.digikey.com/en/products/detail/te-connectivity-linx/BAT-HLD-001-THM/3044009?_gl=1*10no8pn*_up*MQ..&gclid=Cj0KCQjwztOwBhD7ARIsAPDKnkAVl-omgrW-V7a-AVtoaE2QZEPQHywOrfch-0X9evkTW-sQ3L3zPZgaApR6EALw_wcB)

## Real-Time Clock

In order to have a RTC, an external battery must be included to provide VBAT.

The uC has a battery charging circuit and can be activated when VDD is present.

LSCO pin

OSC32\_OUT pin provides clock?

OSC32\_IN and \_OUT ports can supply input to the LSE clock used to generate the 1-second clock for RTC. A crystal, resonator, or oscillator can be used to provide the signal.

Crystal used by them in AN5156 is [MU00137-32.768K](https://www.digikey.com/en/products/detail/ndk-america-inc/MU00137-32-768K/9172005).

## Character Display

The ability to power and write to a small character display is made available by exposing the pins needed. The display chosen as a reference is the [C204A-FTW-LW63](https://focuslcds.com/product/c204a-ftw-lw63/) from FocusLCDs, which is a 20x4 character display with backlight. It uses a 3.3V input and a 4 or 8-bit interface. It is roughly 3.9 by 2.4 inches. The pinout is given in the datasheet and uses a 1 x 16 pin header for all data and power pins. The pitch given is 2.54 mm.

In 4-bit mode, only 4 lines are needed to set the character display. The pinout below is taken from the datasheet. However, data is sent in nibbles then so two transactions are required to write data or a command. The FocusLCD [website article](https://focuslcds.com/journals/break-down-of-a-parallel-interface/?srsltid=AfmBOopbbiziXuHUgvugt_7WjOh3LS8rwjkJNCKrJj8tgkYwGZSwBcBg) links the [embeddedcraft.org](http://www.embeddedcraft.org/lcd4bit.html.) tutorial on 4-bit operation. In general, it is indicated that to write two nibbles the data must be set and followed with a pulse on the enable line a total of two times.

A screenshot of a computer

Description automatically generated

The V0 pin is used to modify the contrast of the screen. The [application note](https://focuslcds.com/journals/application-notes/adjusting-the-contrast-of-an-lcd-module/) by FocusLCDs indicates that V0 should be wired to a voltage divider or potentiometer of 10k.

<https://www.mouser.com/ProductDetail/Amphenol/N6L30T3N-103-3030?qs=Rp5uXu7WBW%252B8ZM8WtY2TfQ%3D%3D>

[3362P-103LF-ND](https://www.digikey.com/en/products/detail/bourns-inc/3362P-1-103LF/1088412?gclsrc=aw.ds&&utm_adgroup=General&utm_source=google&utm_medium=cpc&utm_campaign=PMax%20Shopping_Supplier_Bourns_0118_Co-op&utm_term=&utm_content=General&utm_id=go_cmp-20514526774_adg-_ad-__dev-c_ext-_prd-1088412_sig-CjwKCAiApY-7BhBjEiwAQMrrEU76IqBgOSEPhYpK4WGT8y8cJTD9Fkq2F86J8jaD4lm-cdVP529cSRoCV1gQAvD_BwE&gad_source=1&gclid=CjwKCAiApY-7BhBjEiwAQMrrEU76IqBgOSEPhYpK4WGT8y8cJTD9Fkq2F86J8jaD4lm-cdVP529cSRoCV1gQAvD_BwE&gclsrc=aw.ds) is a good potentiometer.

A simple display able to display characters is appropriate for this design. It is expected that an RGB/parallel interface will not be native to the STM32 line so a SPI-based display is an acceptable interface.

One display that could be appropriate for the application is a character LCD display from FocusLCDs (C204AS-FTW-LW63 - [focuslcds.com](https://stg-focuslcds-staging.kinsta.cloud/product/c204as-ftw-lw63/)). This display is transreflective, meaning it should not require a backlight.

A larger, 40 x 4 chararacter display, that is also transreflective is the [C404A-FTW-LW63](https://focuslcds.com/product/c404a-ftw-lw63/) from FocusLCDs which retail for about $30. It also utilizes the parallel connection. It uses a 2x9 set of vias with standard 2.54mm pitch. The backlight typically uses 60 mA but up to 120 mA with 2-3 mA for the digital side.

Character LCD displays contain 14 pins if no backlight is attached ([focuslcds.com](https://focuslcds.com/journals/intro-to-lcd-display-programming-character-lcds/#:~:text=Character%20LCD%20displays%C2%A0contain,displays%2C%20so%20pay%20attention!)). There are 8 data pins, an enable signal, a R/W pin, register select, and 3 power pins. If necessary, 4 pins can be used instead of 8 for data lines.a

<https://www.digikey.com/en/products/detail/nidec-components-corporation/ST4ETA103/738497?gclsrc=aw.ds&&utm_adgroup=&utm_source=google&utm_medium=cpc&utm_campaign=PMax%20Shopping_Product_Low%20ROAS%20Categories&utm_term=&utm_content=&utm_id=go_cmp-20243063506_adg-_ad-__dev-c_ext-_prd-738497_sig-Cj0KCQjws-S-BhD2ARIsALssG0bbxc33rdyjDCcY70kuDJXeHUlZ15IlzaAUOznkSt0WkhV7ywvJwEgaAlJhEALw_wcB&gad_source=1&gclid=Cj0KCQjws-S-BhD2ARIsALssG0bbxc33rdyjDCcY70kuDJXeHUlZ15IlzaAUOznkSt0WkhV7ywvJwEgaAlJhEALw_wcB&gclsrc=aw.ds>

## Antenna Tuning Ready

The device should support the ability to tune the antenna using data gathered from testpoints or usage. The recommended antenna to use is the inverted-F antenna, which will have a fixed design but might be able to be tuned using the matching components.

## Bootloader from Serial Memory

The design should plan to use a bootloader to flash new firmware. The firmware should ideally be located in serial memory and use CRC-32 or alternatives to verify the image.

Creating a bootloader requires creating 2 projects, one for the bootloader and one for the application. Flash memory in the uC needs to be divided between the two programs.

uC Details:

Flash is organized into 4 Kbyte pages. Each page is made of 8 rows of 512 bytes. Page 0 starts at 0x0800 0000 and spans to 0x0800 0FFF. The page number is used in the software procedure to erase a page. Page erase time is ~22 ms and max programming time for 1 Mbyte is 11 ms. The granularity in the standard mode is 8 bytes.

Flash is shared between the M4 and the M0+ core.

Program and erase operations are only possible in power range 1 ().

## Audio Output

Enabling audio output can be done in various ways with various degrees of complexity. At a most basic level, a piezo buzzer can be used with a PWM input to generate sound. A more middle-ground solution would be to utilize the STM to handle some audio processing with custom audio samples and generate the analog signal directly to an amplifier to a speaker. The most complex solution would be having an audio codec chip on board, which handles a wide array of inputs/outputs as well as settings and controls.

Adding audio to the application is a nice value add but having an audio codec is out of the scope of the project. A piezo buzzer is also very simple and can be integrated with little additional work, but also with very little configurability and poses little challenge to the designer. Thus, a solution using the STM32 chip to play short audio samples / beeps / messages seems most appropriate. While adding an audio codec to increase system flexibility would be a great feature add, it would also introduce cost as well as add lots of design/config/testing time due to the increased complexity.

The simplest implementation using the STM32WB would be to only support a mono file and single speaker. Supporting stereo would require more power, components, as well as DAC outputs, and memory to store samples. Having stereo does not add a lot of value to the design/use experience beyond factoring in the additional power requirement.

An example 16-bit mono track sampled at 44.1 kHz for 1 second takes up about 86 kB. Thus, a FLASH chip to store the data is required to store even short samples.

It is noted that it seems to be the recommendation for the audio amplifier to have a power output that is at or just above the rating of the speaker ([reference](file:///C:\Users\jakob\Library\CloudStorage\GoogleDrive-jak.kapala@gmail.com\Other%20computers\My%20Computer\8.0\projects\ble_module\amplifiers)). If the amp is underpowered, it could cause clipping and damage to the speakers. Likewise, too high a power output rating can also damage speakers. A general strategy is to use an amp that is rated for 75% to 150% of the speaker’s power output.

Another important attribute of the audio chain is sensitivity of the speakers, which is a measurement of how efficient a speaker is when converting power into volume. Around 87 db is considered standard for most loudspeakers.

For this application, a target bit depth of 16 is preferred.

### Design Options

The audio chain has some important design factors to consider. These include the digital-to-analog conversion stage, amplification stage, and speaker selection. In general, the conversion happens via a DAC either inside the microcontroller or via an external one. Since the STM32WB does not have an onboard DAC, an external DAC will be used. It should be noted that audio DACs will typically have an Inter-Integrated Circuit Sound (I2S) to streamline communication of the audio sample data to the DAC.

The I2S protocol is a serial interface protocol that is used for transferring two-channel, digital audio as pulse-code modulation (PCM) between two ICs. It was first designed by Philips Semiconductor, now known as NXP Semiconductors, in 1986. It uses three lines to transfer data, 1) a data clock, 2) a left-right channel / word select, and 3) a serial data line. A value of 0 on the word select line will send data to the left channel, a value of 1 sends data to the right channel.

After the signal is generated via the DAC, the audio must be amplified to support the power needs of the downstream speaker. This is done via an audio amplifier, which typically fall within the A, B, AB, or D classes. The different classes provide different benefits that relate to power efficiency, noise generation, EMI, and supply configurations. Class D amplifiers are the most efficient generally but does add switching noise due to the central architecture. For battery-powered applications, Class D is probably the most appropriate.

Browsing on Digikey or Mouser shows that some low-end DACs and amplifiers can be acquired or $1-3, but options are few. One such DAC the [ES9023P](https://www.mouser.com/ProductDetail/ESS-Technology/ES9023P?qs=sPbYRqrBIVn%252BcPkDS1h3%252BQ%3D%3D&srsltid=AfmBOorCMcTxVYMyqf4S6Ji0nHnvsG7kguJZSmwmWppDsx8XpjyiHKZu) from ESS Technology, which is cost-effective and simple to integrate for audio applications. However, its ground-centered output emphasizes a key factor in the audio chain: if the signal is ground-centered or not. In simple terms, the DAC employs an internal charge pump to generate both positive and negative voltages centered around ground to create the analog signal. A major benefit of this is that a DC component is *not* added to offset the analog signal for systems that are operating strictly above ground. It appears this reduces components required in the audio chain, offers better noise performance, but also requires that downstream amplifiers use a bipolar supply. Generating a bipolar supply is not trivial and adds additional cost.

As pointed out, it is important that the DAC and amplifier use the single-supply constraint with a DC offset or bipolar supply. Available low-cost amplifiers like the TS4962IQT appear geared towards the single supply setup, leading to a mismatch at the input. If the ES9023 is used and the output is centered around ground, the TS4962 will be incompatible because the VCC range would be from 0-3.3 or 5V.

Another important characteristic is whether the analog lines are differential or single-ended. It appears that some DACs or codecs could provide differential signaling to handle interference better. Amplifiers like the TS4962 allow for both configurations.

When choosing a speaker, the impedance of the speaker and the power rating must be matched to the amplifier to ensure proper operation. It is recommended that the amp support a higher power rating, one that is less is said to cause audible defects like clicks or pops and at worst could cause damage.

### Integrated DAC and Amplifier

Due to the minimal requirements of the audio system as it is a secondary priority to Bluetooth functionality, cost and ease of implementation led me to selecting the [TAS2505](https://www.ti.com/product/TAS2505-Q1) from Texas Instruments as DAC + amplifier block. It supports mono audio and received data over analog or I2S, providing up to 2W via the class D amplifier. It is a more recent chip, originating in 2017. I2S and SPI can both be used to interface with internal controls and is packaged in a 24-pin VQFN chip. Bit depths of 16, 20, 24, or 32 bits are supported.

It does require a 1.8V rail to supply AVDD and DVDD. The IO level can be set by IOVDD and can range from 1.1 to 3.6V, allowing for compatibility with the STM32WB IO. An additional power pin, SPKVDD, sets the power of the final stage and ranges 2.7 to 5.5V.

The device does have an internal LDO that can be used to generate AVDD and DVDD from an input range of 2.7 to 5.5V with high PSRR. It does have a dropout voltage of 300 mV and can support load currents up to 50 mA. This is optional however. If the LDO is used, then AVDD should be connected to DVDD externally as the LDO does not connect internally to DVDD.

A single-ended headphone output is also available.

The analog inputs, since they are not used, are tied together per the note from the datasheet.

The DAC requires a CLK signal fed in from the MCLK, BCLK, or GPIO/DOUT pins. The on-chip PLL can also be used to generate the required clocks from a wide range of fractional multiplication values to set.

Texas Instruments has provided an application reference [guide](https://www.ti.com/lit/ug/slau472c/slau472c.pdf?ts=1740604691643) to aid in using the device.

A diagram of a circuit

AI-generated content may be incorrect.Additional information that is useful is provided by an applications engineer on the Texas Instruments [forums](https://e2e.ti.com/support/audio-group/audio/f/audio-forum/703441/tas2505-output-lc-filter-calculation) when discussing the output filtering stage. The typical switching frequency is 300 kHz and the min/max is 250/350 kHz, using BD modulation. An engineer in another [post](https://e2e.ti.com/support/audio-group/audio/f/audio-forum/979784/tas2505-q1-low-pass-filter-for-8ohm-speaker-requirements) confirms that a low-pass filter is not mandatory to drive an 8-ohms load, but that it is possible to add an LC filter in order to eliminate EMI noise and provides a link to an [application report](https://www.ti.com/lit/an/slaa701a/slaa701a.pdf) “LC Filter Design”. The report indicates that for BD modulation, type-2 filter can be used. Through some change of perspective of the schematic components, a differential speaker and filter can be modeled as a single-ended one where the load is halved. It is confirmed in another [post](https://e2e.ti.com/support/audio-group/audio/f/audio-forum/812319/tas2505-q1-output-signal-question) that the output without a filter is a PWM signal, not the analog signal you might expect for audio.

Figure 2: BTL Differential Speaker

A diagram of a circuit

AI-generated content may be incorrect.Following the report the component values for a filter can be calculated. Let , where . The parameters from the system are , , and . Solving for L yields that . The capacitor value can be calculated via . The next closest standard value is 0.68 uF, so that will be chosen.

Figure 3: Equivalent Single-Ended Circuit

The document notes that both metalized film capacitors and ceramic capacitors are used in high-power designs. Metalized film types are recommended over ceramic caps due to performance across temperature, voltage, current, and frequency but it is noted that ceramics can be used in space-constrained designs. Agreeing with this sentiment, it is recommended by [EE Times](https://www.eetimes.com/understanding-output-filters-for-class-d-amplifiers/#:~:text=Ceramic%20capacitors%20experience%20large%20changes%20in%20capacitance%20as%20the%20voltage%20across%20them%20changes%2C%20which%20can%20result%20in%20distortion.) to not use ceramic capacitors because of their derating with increasing voltage applied. This factor is dependent on the voltage applied and capacitor voltage rating. Texas Instruments notes that a guideline equation of can be used to estimate the expected capacitor value in the system. Thus, a 100V rated capacitor experiencing 50V volts will derated by 50%. The total voltage experienced over a capacitor can be estimated using . Given the expected system parameters, , , . This gives an expected voltage over the capacitor, . Typical voltage ratings for 0603 packages include 16V, 25V, 35V, and 50V. This gives a range of derating starting from 29% to 9% percent. This will move the cutoff point for the LP filter to a lower frequency, attenuating higher frequency signals. An additional 0.1 uF in parallel with each main capacitor could add the capacitance lost due to derating.

The TAS2505 has both standby and shutdown modes available. When powered by two buses, one for the speaker and another for the 1.8V DVDD and AVDD inputs, standby can be triggered by disabling internal registers. These include the following register blocks, as indicated by a [post](https://e2e.ti.com/support/audio-group/audio/f/audio-forum/970509/tas2505-question-for-power-saving-mode) on the TI forums:

1. DAC Channels (page 0 / register 63 / bit D7)
2. Master reference (page 1 / register 1 / bit D4)
3. Headphone output and analog inputs (page 1 / register 9 / bits D5, D1, D0)
4. Speaker Class-D driver (page 1 / register 45 / bit D1)

A full shutdown can be achieved by turning of all external supplies ([source from TI forums](https://e2e.ti.com/support/audio-group/audio/f/audio-forum/849669/tas2505-about-standby-mode)) and IOVDD can be turned off before the rest of the power is cut. The [application reference guide](https://www.ti.com/lit/ug/slau472c/slau472c.pdf?ts=1742237505640) indicates that technically SPKVDD should be provided first, then IOVDD, then AVDD/DVDD but there is no required minimum time. There is a 10 ns time between when DVDD is provided and the reset pin can be raised.

We can leave I2C pulled high but not sure if IOVDD needs to be cut.

The interrupt signals INT1 and INT2 can be configured, but it looks like I only need one. Map to DOUT/GPIO.

MAP GPIO to LED? Map INT1 to MISO for ease of routing.

TIDA-01529 is the evaluation board and shows that only a capacitor of 1 uF, 50V rating, is needed for AINL and AINR inputs. The evaluation board used RCA mono connectors, specifically the 971 and [972](https://www.digikey.com/en/products/detail/keystone-electronics/972/317317). Based on the schematic of the part, the signal is fed to the center socket pin.

<https://product.tdk.com/en/techlibrary/applicationnote/d-map_suppression-filter_esd-notch.html>

ACDL2V0910-100-R

[VLS6045AF-220M](https://www.mouser.com/ProductDetail/TDK/VLS6045AF-220M?qs=lc2O%252BfHJPVaPRXMBSSNqgw%3D%3D&srsltid=AfmBOoqoBHSDos2Jw7-xeLaVVWG6lAadANva46ijgBBG4CJSoYLb-C7Y) – 22 uH, shielded, TDK

AVRF060X100LT242 – Filter ESD for BLE / Wifi

### Speaker Selection

The speaker should be an 8 ohm-rated speaker with a small footprint to be compatible with the amplifier stage output, which can output up to 1.7W when SPKVDD is 5.5V. The [CMS-151135-078S](https://www.sameskydevices.com/product/audio/speakers/miniature-(10-mm~40-mm)/cms-151135-078s-67?srsltid=AfmBOoqTfnCTGYd3LyVLHlCBrfSWOTk-Qs2GJ4QNf1zjys667iJjuh24) is a 0.7W, 8 ohm speaker. In comes in a 15 x 11 x 3 mm package and is readily available at Mouser and Digikey for around $2.30. It supports a frequency range of 100-20 kHz, which covers most of the audible range for music. The bass range is lacking a bit, as the frequency range for audio is generally quoted as being from 20 Hz up to 20 kHz. This is acceptable, however.

The resonant frequency of a speaker also has an important part in the design. The [post](https://blog.miscospeakers.com/understand-resonant-frequency-and-speaker-design) “Understand Resonant Frequency and Speaker Design” by Misco provides a quick brief on how a speaker’s resonant frequency will affect design and performance. The speaker will operate the most efficiently close to its resonant frequency, any frequencies below this are not easily produced and may not come through.

The speaker has spring contacts that need to mate to the positive and negative terminals of the TAS2505 output. As there is no additional mounting features, a solution using adhesive or a 3D printed frame will be used to enable mounting.

An alternative variant of the same speaker utilities different wired connectors such as from Molex (Molex 51021-0200) or JST (JST SHR-02V-S-B). In order to provided additional flexibility, a Molex connector (0532610271) is included with jumpers to allow for a wired variant.

Other speakers readily available on Amazon, Adafruit, Digikey, etc generally seem to either come with bare wire leads or use the JST-PH type of connector with pitches either at 1.25mm, 2.0mm, 2.5mm or 2.54mm.

Pin 1 is usually the ground/negative wire for the small 2-pin connectors.

CMS-151135-078S with spring contacts

[CMS-151103-088SP](https://www.cuidevices.com/product/resource/cms-151103-088sp.pdf)

CMS-241535-078L65 – 0.7W, 8 ohm, 1.25mm

CMS-30204-18L250 – 1W, 8 ohm, 2.54 mm

Zhenliang Electronic XH-2A – 2.54 mm for CMS-3047-18L300 (1W)

1.25 mm port – Molex PicoBlad 1.25 mm

JST-PH2.0 interface

### DAC

The STM32WB does not have an onboard DAC so a DAC will have to be provided. It makes sense to use a 16 bit chip to support 16-bit audio playback, except most DACs readily available on Mouser and Digikey start around $5, an example being the [DAC8551](https://www.digikey.com/en/products/detail/texas-instruments/DAC8551IADGKR/1509340).

Not all DACs are built the same however, so an audio DAC is most appropriate. One such example that is also cost effective, as of writing, is the [ES9023P](https://www.mouser.com/ProductDetail/ESS-Technology/ES9023P?qs=sPbYRqrBIVn%252BcPkDS1h3%252BQ%3D%3D&srsltid=AfmBOorCMcTxVYMyqf4S6Ji0nHnvsG7kguJZSmwmWppDsx8XpjyiHKZu) from ESS Technology. It includes an integrated 2 Vrms op-amp driver. It is noted that if a smaller bit-width is used, the remaining is zero-padded so sending 16-bit data should be ok. It uses Inter-Integrated Circuit Sound (I2S) as the data interface. However, the device also requires a master clock for internal synchronization, which is the case with other options such as the [AK4432](https://www.akm.com/content/dam/documents/products/audio/audio-dac/ak4432vt/ak4432vt-en-datasheet.pdf). Thus, the STM32WB will need to provide a clock signal.

The DAC will output a signal between 0 and 3.3V based on the data it receives over I2S. There are no additional controls provided over SPI or I2C.

#### I2S Protocol

The I2S protocol is a serial interface protocol that is used for transferring two-channel, digital audio as pulse-code modulation (PCM) between two ICs. It was first designed by Philips Semiconductor, now known as NXP Semiconductors, in 1986. It uses three lines to transfer data, 1) a data clock, 2) a left-right channel / word select, and 3) a serial data line. A value of 0 on the word select line will send data to the left channel, a value of 1 sends data to the right channel.

### Audio Amplifier

The audio amplifier is responsible for boosting the strength of the signal from the DAC so that it can be fed into a speaker. There are different classes of amplifiers to choose from, the main types being A, B, AB and D. Class D amplifiers are becoming more popular due to their efficiency. One option identified is the TS4990IST from STM, which is a low-cost 1-channel class AB amplifier.

In general, it seems that most amplifiers are only able to provide at max about 500 mW for an 8 ohm load with a 3.3V input. To provide more power, 3.6V or 5V is typically referenced in datasheets. Thus, a reasonable candidate for an amp is the TS4962.

Other options:

[IS31AP2005-DLS2-TR](https://www.digikey.com/en/products/detail/lumissil-microsystems/IS31AP2005-DLS2-TR/2863802)

TPA2006D1DRBR

TS4990IDT

TS4962IQT – class D,

One such example that is also cost effective is the [WM8523](https://www.mouser.com/datasheet/2/76/cirr_s_a0009574211_1-2263154.pdf) from [Cirrus Logic](https://www.mouser.com/ProductDetail/Cirrus-Logic/WM8523GEDT-R?qs=3xHz9%2FyNEPiU17QOvk1mXA%3D%3D). It takes in an I2S line for the data and is controlled via I2C or SPI. It supports stereo mode.

OPTIONS:

AK4432VT – 400 kHz I2C, 3.3V

TPC112S1-VR

[MCP48CVD11-E/MF](https://www.digikey.com/en/products/detail/microchip-technology/MCP48CVD11-E-MF/16709754) – 10 bits, SPI

[MCP48FVB21-E/UN](https://www.digikey.com/en/products/detail/microchip-technology/MCP48FVB21-E-UN/5773466) – 12 bits, SPI

[MCP48CVD21T-E/MF](https://www.digikey.com/en/products/detail/microchip-technology/MCP48CVD21T-E-MF/16709741) – 12 bits, SPI

[TAD5142IRGER](https://www.mouser.com/ProductDetail/Texas-Instruments/TAD5142IRGER?qs=%252BXxaIXUDbq2O3ZqznkiERg%3D%3D)

[ES9023P](https://www.mouser.com/ProductDetail/ESS-Technology/ES9023P?qs=sPbYRqrBIVn%252BcPkDS1h3%252BQ%3D%3D)

<https://www.mouser.com/ProductDetail/Cirrus-Logic/WM8523GEDT?qs=3xHz9%2FyNEPivjlX0hknU6A%3D%3D>

### Audio Amplifier

The Class-D amplifier chosen is…

TPA2005D1-Q1, class D, 0.75W at 8 ohms

[TPA711DGNR](https://www.digikey.com/en/products/detail/texas-instruments/TPA711DGNR/374588) – 0.7W at 8 ohms at 5V, NO

TS4990IST – 500 mW at 3.3 for 8 ohms – I like this one, good datasheet.

LM4861MX/NOPB

Reading out the sample will need to happen over an I2C or SPI bus. The paper “[Common Inter-IC Digital Interfaces for Audio Data Transfer](https://www.analog.com/media/en/technical-documentation/technical-articles/ms-2275.pdf)” by Analog Devices states that I2S, a very popular audio IC-IC transfer protocol, uses a typical clock rate of 512 kHz for an 8 kHz signal and 12.288 MHz for a 192 kHz sample rate.

A timer will be configured to operate at the specified sampling frequency to change the DAC input.

The STM32WB supports both DMA and QSPI which can speed up reading from an external device.

Memory-mapped mode allows external flash memory to be seen by the system as if it were an internal memory.

A possible speaker to implement would be the [CMS-151103-088SP](https://www.cuidevices.com/product/resource/cms-151103-088sp.pdf). It is rated at 0.7W with 8 ohm impedance, up to 1W. This means the typical voltage level should be ,

The Serial Audio Interface sends data from memory (local or external) to an audio codec chip, which then drives a DAC output into an amplifier. Common bit depths include 16 bit, 24 bit.

Can use following audio protocol:

* I2S, LSB or MSB justified
* PCM/DSP
* TDM
* AC’97
* SPDIF out

### Audio Codec IC

To convert the file format to a useable input code by a DAC, an audio codec chip can be used. The chip handles interpreting the file format and standardizing the output to digital codes for the DAC. To have stereo sound, two channels must be output to a DAC(s) and amplifiers.

|  |  |  |  |
| --- | --- | --- | --- |
| **Device** | **Manufacturer** | **Price** | **Description** |
| [SGTL5000XNLA3](https://www.mouser.com/ProductDetail/NXP-Semiconductors/SGTL5000XNLA3?qs=sGAEpiMZZMuGeGLVV4AlaXDPLJJLEwgRW5gQ9lWdOP0%3D) | NXP Semiconductors | 3.66 | 24 bit, 96 kHz, I2C / SPI, 1.62 to 3.6V, 1 channel |
| [6PAIC3109TRHBRQ1](https://www.mouser.com/ProductDetail/Texas-Instruments/6PAIC3109TRHBRQ1?qs=sGAEpiMZZMuGeGLVV4Alaei%2FfOAnaxFBlBkUBMqGygE1TN2pwhvlNw%3D%3D) | Texas Instruments | 3.52 | 16 bit, 96 kHz, I2C, 1.8 / 3.3V, mono, 1 channel |
| [TLV320AIC3101IRHBR](https://www.mouser.com/ProductDetail/Texas-Instruments/TLV320AIC3101IRHBR?qs=sGAEpiMZZMuGeGLVV4AlaUH1mFnnbOAhadf13BMDy2U%3D) | Texas Instruments | 3.00 | Multiple bit rate, stereo 8 ohm 0.5W speakers supported, |

[TLV320DAC3203IRGER](https://www.mouser.com/ProductDetail/Texas-Instruments/TLV320DAC3203IRGER?qs=sGAEpiMZZMuGeGLVV4AlaY1ReVQJEZKAR%2F152BtTwt8%3D)

[TLV320AIC3101IRHBR](https://www.mouser.com/ProductDetail/Texas-Instruments/TLV320AIC3101IRHBR?qs=sGAEpiMZZMuGeGLVV4AlaUH1mFnnbOAhadf13BMDy2U%3D) – 8 ohm, 0.5W output

[**TLV320AIC3100IRHBR**](https://www.digikey.com/en/products/detail/texas-instruments/TLV320AIC3100IRHBR/2193085), has beep generator, can power a 4 ohm differential load

A note on audio outputs: there are sometimes any configuration of three outputs in audio chains. These include:

1. Speaker output, such as Class-D
2. Headphone output
3. Lineout

A lineout is typically being fed to a driven load, meaning it does not have to source as much current as a channel would for a headphone. Headphones are driven directly from the output, so the output impedance should be low and source ample current. The speaker output drives a speaker directly, sourcing the current needed while using the analog voltage from a DAC to construct the source signal.

To avoid audible hiss from amplifier noise floor, SNR in a class-D amp should exceed 90 dB in low-power amplifiers ([Analog Devices source](https://www.analog.com/en/resources/analog-dialogue/articles/class-d-audio-amplifiers.html#:~:text=Signal%2Dto%2Dnoise,satisfactory%20overall%20SNR.)).

Can any speaker use differential or single ended?

[**TAC5142**](https://www.ti.com/product/TAC5142)

## Piezo Buzzer or Speaker

PWM can be used to generate a square wave, which is then run through a LPF to round the corners.

[CEP-2224](https://www.cuidevices.com/product/resource/cep-2224.pdf), 3-20 VDC, internal drive – NO, for 12V

[AI-3035-TWT-3V-R](https://www.digikey.com/en/products/detail/pui-audio-inc/AI-3035-TWT-3V-R/1745457), 2-5 VDC, internal drive

[PS1240P02BT](https://www.digikey.com/en/products/detail/tdk-corporation/PS1240P02BT/935924), 0-30 V, external drive, zero-peak signal

## USB

The STM32WB series offers a full-speed (FS) USB 2.0 interface, 12 Mbit/s. Up to 16 endpoints are supported.

The connector appropriate for the design is a USB 2.0 connector, which does not route the additional USB 3.0 pins. This reduces pin count and soldering complexity. The primary pins that are routed are the standard D+, D-, CC1, and CC2 pins. The SBU pins, the sideband channels, that are available through the connector should be left floating as they are not used. These are used in other protocols supported by the USB-C technology such as Audio Adapter Accessory Mode, USB4, Thunderbolt, or HDMI.

The shield is connected to ground, per USB-C specifications.

The USB data lines, D+ and D-. should be routed as a differential pair. The trace impedance should be matched to the cable impedance, which is set around 90 ohms. This [document](https://www.ti.com/lit/wp/slyy109b/slyy109b.pdf?ts=1743131061614&ref_url=https%253A%252F%252Fwww.google.com%252F) by Texas Instruments indicates that the specification allows for connecting of the D+ and D- pairs directly. Some designs elect to use a USB 2.0 Mux to improve signal integrity when merging the pairs. The [article](https://resources.altium.com/p/routing-requirements-usb-20-2-layer-pcb#:~:text=Differential%20Skew,is%20very%20large!) “Routing Requirements for a USB Interface on a 2-Layer PCB” by Altium notes that for High Speed USB, which is faster than the Full Speed, should allow for about 600 mils (15 mm) of length mismatch.

The [application note](https://www.st.com/content/ccc/resource/technical/document/application_note/group0/0b/10/63/76/87/7a/47/4b/DM00296349/files/DM00296349.pdf/jcr:content/translations/en.DM00296349.pdf) “Introduction to USB hardware and PCB guidelines using STM32 MCUs” by STM indicates that no serial termination resistors are needed on the data lines.

There is a USB\_NOE output port which indicates if the USB transceiver is active. While useful, it is not necessary and not implemented because it would interfere with the JTAG pins.

There is also a USB\_CRS\_SYNC output which is related to the clock recovery system and can be used as a trigger in a fine tuning process for the 48 MHz frequency. It will not be utilized as other inputs include the 32 kHz crystal oscillator and USB Start of Frame signals.

A screenshot of a computer

AI-generated content may be incorrect.USB data lines (D+, D-) should be impedance matched to 90 ohms differential. A trace width of 16.65 mils with spacing of 8 mils should accomplish this on the basic JLC04161H-7628 stackup.

The CC tracks should be 10 mil to provide enough current capacity for supported cables, per the datasheet (9.4.1.5).

As I have filled the top of the board with ground, but my USB data routing is using a coupled microstrip mode, the top-layer ground should be pulled back around the USB traces to avoid coplanar waveguide effects. The Altium [article](https://resources.altium.com/p/microstrip-ground-clearance-how-close-too-close), “RF Microstrips and Ground Plane Clearance: How Close is Too Close?” notes that a field solver is required to recommend a separation distance but concludes that a rule of 3W is generally too conservative. An example given is that for a microstrip trace of 12 mils, a separation distance of 36 mils should be used to pull back the ground planes surrounding the strip. Here my mode is a coupled microstrip where each line is 16.65 mils wide, so the separation from ground could be 48 mils.

https://resources.altium.com/p/differential-microstrip-impedance-calculator

https://resources.altium.com/p/routing-requirements-usb-20-2-layer-pcb

## Current Monitoring

The board supports current monitoring on a few power lines using a sense resistor and connected ADC. The points monitored include:

1. System monitoring through VBUS sensing
2. **Placeholder**

#### VBUS Monitoring ✅

The accuracy of the current sensing comes down to maximizing the sense resistance while limiting the power dissipation in the resistor and offset error and reduced common-mode rejection due to bias currents. A recommendation from Texas Instruments for their INAx180 line is to keep sense resistors no larger than a few ohms.

Power dissipation is governed by . 5A is the maximum allowed over USB-C lines. While I expect the working current to be much less, entirely bounded by the more standard 3A limit, I want to design the sense circuit to have some overhead. I will somewhat arbitrarily choose a max current of 6.3A. Damage to the circuitry will probably occur if this current is actually drawn but since it is governed by USB PD it shouldn’t be allowed anyways. A minimum current could be estimated to be 50 mA, for the purpose of the following calculations.

A good option for the current sense amp is Texas Instruments’ INAx180 series, which supports both high side and low side sensing. In this case, we are using high side sensing since the resistor is placed directly after the USB port and sees the VBUS voltage. The INAx180 has options for gains of 20, 50, 100, and 200 V/V and common mode voltages up to 26V. It does support a shutdown mode by removing the power to the power pin, though this isn’t required.

If we suppose that the max current through the resistor is 6.3A then the relationship becomes . If a 1W resistor is used, then . Thus, the initial choice is 25 mOhm.

An additional requirement is to make sure that the output voltage does not swing past the allowed rails by verifying the gain selection. The TI datasheet provides the following guidelines to verify the selection. and are given in the equations and refer to the positive and negative swing values and are provided in the datasheet in section 7.5.

If a gain of 20 is chosen, the relationships are satisfied.

At 1A drawn, power dissipation should be .

If 5A is drawn, the voltage seen over the resistor should be , which then gets amplified to

A final output voltage to the system of 4.875V should be acceptable since it will get stepped down to 3.3V later anyway.

[ERJ-8CWFR025V](https://www.digikey.com/en/products/detail/panasonic-electronic-components/ERJ-8CWFR025V/4927007) is a good option for the sense resistor that is 25 mOhm with a power rating of 1W in a large 1206 package.

[INA180A1IDBVR](https://www.digikey.com/en/products/detail/texas-instruments/INA180A1IDBVR/8132986) is the appropriate model to have a gain of 20 in an SOT-23-5 package. It supports a power supply voltage of 2.7 – 5.5V to power the device. The datasheet also indicates that the device can be powered down using a logic gate or switch to drive the VS pin. Current leakage when the device is off but common mode voltage is present is said to be dictated by the bus voltage and 500 kOhm impedance in the device to ground. Small leakage should be acceptable for the short amount of time the device is unpowered.

## Temperature Monitoring

The footprint for a temperature monitor is included to provide additional functionality. The TMP1075 has an alert pin that can operate in two modes to indicate significant states in the system. The comparator mode will activate the alert pin if the temperature measured is out of the high and low bounds. The interrupt mode will sound the alert if temperature rises above the high setpoint and will sound again when the temperature falls below the low setpoint.

Note that the temperature measured could be greatly effect by heat generated from circuit elements. The application [report](https://www.ti.com/lit/an/snoa967a/snoa967a.pdf) “Temperature sensors: PCB guidelines for surface mount devices” by Texas Instruments discusses this issue and ways to address it.

The device supports up to four addresses depending on the state of the A0 pin. Tying it to ground sets the 7-bit address to 1001 000.

## EMI/EMC

Without specialized tools, internal testing will be limited. The design should utilize best practices, use simulations where possible, and design in test points if they are applicable. In lieu of test results from the assembled system, a route to perform tests should be provided. This includes any tests that could possibly be down internally with the addition of an inexpensive tools and where to send the device for external tests.

### EMI Practices

In order to mitigate EMI, various techniques are used to target common sources of emissions. These are discussed below in various details depending on how specific they are to this design and what block they apply to.

Large capacitances can react with impedances to create resonances.

#### Reference Change Vias

Vias are placed by nearby signal vias to allow the signal reference to change from the L2 to L3 ground plane.

#### Serial Termination Resistors on High-Speed Lines

One common source of EMI is through mismatched impedances of a driver, the transmission line, and the load. A driver could be an output clock from a microcontroller and a load could either be another IC for memory or sensing. Typically, the driver will have an impedance in the range of 10s of ohms, the transmission line will be matched to around 50 ohms, and a load will have a high impedance in the kOhms/mOhms region. This mismatch creates reflections, which causes signal integrity and EMI issues. The reflection % is given by . If then a positive reflection occurs, where the reflection is added to the base signal, and overshoot occurs. The opposite case is undershoot, where reflection subtracts from the signal. In today’s digital domain and architecture, undershoot is more of the problem due to lower digital rails, noise margins, so generally it is recommended to err on the side of designing for overshoot.

When traces are sufficiently long and the frequencies on the trace are fast, antennas can be formed as the length of the antenna depends on the wavelength of the signal. Fast signal means shorter wavelength, allowing for shorter antennas. The issue can present itself in unexpected circumstances, as a relatively lower clock signal might not catch the designer’s attention if they neglect to consider the edge rate of the signal. In general, to create square pulses over a digital line there must be frequencies several times faster than the base frequency in order to create nice transitions. These higher frequencies should be accounted for when analyzing the length of the trace.

The application note [AN4760](https://www.st.com/resource/en/application_note/an4760-quadspi-interface-on-stm32-microcontrollers-and-microprocessors--stmicroelectronics.pdf) from STM references the [AN4661](https://www.st.com/resource/en/application_note/an4661-getting-started-with-stm32f7-series-mcu-hardware-development-stmicroelectronics.pdf) note for layout guidelines. The main takeaways are to design for 50 ohm traces and if the trace is over 120mm then termination is required. Match the data pin lengths to within 10mm of each other, an “S” style serpentine can be used. Do not use serpentine routing on the clock trace and provide at least 3x the trace width away from other signals.

For reference, Phil’s lab provides a brief overview of SI and EMI in this [video](https://www.youtube.com/watch?v=VtzPL8wQ8-E).

Not needed for <10 MHz lines shorter than 10 cm?

#### Audio Circuitry

The audio block should follow this [article](https://www.ti.com/lit/an/snaa050a/snaa050a.pdf?ts=1740599253596) by Texas Instruments. The Class-D amplifier is efficient, a desired trait for low or battery powered systems, but also utilizes switching in the architecture which poses an EMI concern. A couple recommended techniques from the article to combat this include:

* Standard power decoupling practices
* Power planes are backed off from the edge of the PCB
* Adequate termination of all high-frequency clock lines
* Proper filtering of PCB connectors
* Avoid loop antennas, where a forward and return current is on a well-defined conducting path
* Keep audio traces as short as possible

#### Via Fences

This [article](https://www.nwengineeringllc.com/article/designing-your-rf-pcb-stackup.php) explains that via fences around different sections of circuitry can be beneficial.

#### Power Plane Pullback

The [article](https://resources.altium.com/p/ground-plane-design-and-arrangement-high-performance-pcbs) “PCB Ground Plane Design in High Performance Boards” by Altium i

## DFM Check

<https://www.protoexpress.com/blog/dfm-issues-pcb-manufacturing/#:~:text=It%20is%20a%20process%20of,manufactured%20to%20the%20exact%20specifications>.

Minimum trace width

Via min sizes

Clearance from edge is >0.2mm for JLCPCB

## Configuration Details

If SWO is available, select Trace Asynchronous Sw in SYS / DEBUG menu.