BLE Demo Implementation

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# Overview

This document serves as the design output document. It contains details of implementation as well as design choices to match specifications.

# Hardware Design

Based on the design specs, the following hardware design

## STM32 Architecture and related toolchains

### STM32WB / STM32WBA / STM32WB0

The STM32WB line supports multiple wireless protocols. It does not support WiFi though, so Wifi is not available unless another chip is added. The B0 line is the simpler line of the three, the BA lime is the most robust.

The chips run for about $6 to $9 on Digikey. There are a few around $4-5 on Mouser.

STM32WB30CEU5A is a decent option to design with given available peripherals. WiFi and TCP Client with SSL is NOT available on this device, there is no stack for it.

Pin count estimation is given as follows:

* SPI – Serial Memory, 4
* SPI – MicroSD, 1
* JTAG – 4/5
* USB – 2
* Piezobuzzer – 1
* UART – Console, 4
* Character Display – 7 or 11
* LEDS – 2-3

STM32WB35CCU6A is a good option that offers FS USB (2.0) and 30 GPIO.

[Link to Mouser](https://www.mouser.com/ProductDetail/STMicroelectronics/STM32WB30CEU5A?qs=DPoM0jnrROXA98TRXR4iRg%3D%3D).

[Link to Datasheet](https://www.mouser.com/datasheet/2/389/dm00627896-1799525.pdf).

[STM32WB55RCV6](https://www.mouser.com/ProductDetail/STMicroelectronics/STM32WB55RCV6?qs=vLWxofP3U2y%2F21YKkPUpfQ%3D%3D) is a good option for USB and 49 I/O.

## BLE and Inverted-F Antenna

The STM32 has an 32 MHz crystal, per the requirement.

## WiFi and TCP Client

Not supported in the BLE enabled STM32 chips. Thus, it is the decision of the designer to omit this feature from this board.

## DMA Utilization

DMA can be used to move data between two locations quickly without CPU involvement. Priority can be programmed to handle multiple requests across the configurable channels. DMA should be used to configure peripheral-to-memory, memory-to-peripheral, or peripheral-to-peripheral transfers. Transfer size should be flexible.

uC Notes:

Supports transfer size of 2^16. Allows access to flash memory, SRAM, APB, and AHB peripherals. There are 7 independently configurable channels.

## High-Capacity Non-Volatile Memory

The board should both be able to utilize a surface mount memory controller but also have a MicroSD housing to allow the use of external memory chips.

### Serial Memory

NAND Flash offers high memory density for the lowest cost in general. Commonly available sizes include up to 512 MB. For this application, a chip in the 124 MB range would suffice.

<https://www.digikey.com/en/products/detail/winbond-electronics/W25N01GVZEIG/15181734>

<https://www.mouser.com/ProductDetail/Winbond/W25N01GVZEIG-TR?qs=qSfuJ%252Bfl%2Fd6niBi0Qz1MPg%3D%3D>

NOR Flash has a large range of products on Mouser and on Digikey. Common sizes range up to 1 Gbit / 125 megabytes. Micron Technology, Infineon, and Macronix are primary manufacturers of the technology. Like NAND, NOR is erased on blocks such as 4 kbyte. NOR flash is suggested to be more reliable over time and common for permanent storage (compared to SD-card like removeable memory). Costs seems to range around $10-20 for such larger capacity chips.

FRAM and MRAM are both better for endurance and size but are quite expensive. Would require specialized application to utilize benefits.

### microSD Card

There are different types of microSD cards, including:

1. SDSC (Standard Capacity)
   1. Max 2GB
   2. FAT16
   3. Typical max transfer speed of 12.5 MB/s
2. SDHC (High Capacity)
   1. Max 32GB
   2. FAT32
   3. Bus speeds of 12.5 MB/s to 25 MB/s typical, up to 3938 MB/s depending on bus interfaces
   4. Interfaces: UHS-I, UHS-II, UHS-III, SD-Express
3. SDXC (Extended Capacity)
   1. Max 2TB
   2. FAT32 or exFAT
   3. Bus speeds of 12.5 MB/s to 25 MB/s typical, up to 3938 MB/s depending on bus interfaces
   4. Interfaces: UHS-I, UHS-II, UHS-III, SD-Express

In general, SD cards have 9 pins and micro. A standard SD card can operate in 3 modes: 1) SPI, 2) one-bit SD, and 3) Four-bit SD. Cards historically have used 3.3V since their introduction in 2000. Recent additions to the protocol allow cards to use 1.8V levels but may require the controller to initialize the card using 3.3V logic.

MicroSD pinout is standardized, listed below:

|  |  |  |
| --- | --- | --- |
| Pin Number | SD Name | SPI Name |
| 1 | DAT2 | X |
| 2 | CD / DAT3 | CS |
| 3 | CMD | DI |
| 4 | VDD | VDD |
| 5 | CLK | SCLK |
| 6 | VSS | VSS |
| 7 | DAT0 | DO |
| 8 | DAT1 | X |

The mode cannot be switched while power is applied. In this case, the SPI interface is easier to implement. Note also that SD cards must be read/written to in sectors (512 bytes). QSPI is not applicable.

SD cards may or may not have wear leveling available, it depends on the manufacturer.

A filesystem library will be needed to format data to the FAT-formatted card.

## Memory Encryption

To enable encryption on memory,

## JTAG

JTAG is an interface, not a specific function. It can be used for processor debug, programming, and programming. It uses four signals.

Supported by uC. Shared with SWD.

## Power Configuration

The power requirements of the system are primarily driven by the RF components of the board since they are most sensitive. The STM32 is designed for low-power applications running off coin-cell batteries, drawing up to 7.8 mA when the highest power level (+6 dBm). It has an onboard SMPS that can be optionally used given a high enough VDD. It is noted that the integrated LDOs that feed the system, including the RF and digital circuits, can be sourced either from the integrated SMPS or an external source. However, the other subsystems are fed directly from their source.

There are several elements in the STM32 that are powered:

VDD: feeds I/Os, SMPS, RF, internal clocks by 1.71 to 3.6 V.

VDDA: ADC/Comparators fed by 1.62 to 3.6 V.

VDDUSB: for USB transceivers fed by external 3.0 to 3.6 V.

VLCD: for the LCD controller fed by 2.5 to 3.6 V.

There are three embedded regulators that supply most of the digital and RF circuits, the three being the main regulator (MR), low-power regulator (LPR), and the RF regulator (RFR). The MR is used in the run and sleep modes as well as stop 0 mode, the LPR is used in a low-power run/sleep modes as well as stop 1 and stop 2 modes. It is used to power the SRAM2a in standby as well. The RFR supplies the RF analog part. All regulators are powered down in standy and shutdown modes and the outputs go to a high impedance mode.

By default, the microcontroller is in run mode, range 1, after turning on.

### USB-C Bus and PD Controller ✅

The main power bus comes from USB PD.

VBUS has an ESD protection diode, the TVS1800DRV, added for safety. It is [recommended](https://www.ti.com/lit/an/slvaf82b/slvaf82b.pdf?ts=1714998779059) by TI for a PD voltage of 15V.

This board will not support a native battery to the main supply as that is beyond the scope of the design. This is because a common USB-C application would utilize a rechargeable battery which powers the system and USB-C is used to recharge the battery during operation. Thus, the USB-C controller should support the “dead battery” mode, where the device can be powered up with a dead battery state.

The TPS25730 is a decent option with good documentation as well as features to utilize. It supports dead battery mode and uses a resistor divider to set the I2C address as well as voltage min, max, and current bounds. It also contains an integrated protection FET for VBUS. The TPS is powered by VBUS or VIN\_3V3, the latter being the typical supply. Upon registering the dead battery condition, VBUS is used and VIN\_3V3 remains disabled until cleared using I2C. Thus, VIN\_3V3 could be hooked up to receive power from a 3.3V bus when it is available.

Four pins (ADCINx) set the voltage and current capabilities of the PDO to be requested. It is also used to set the I2C address. Since the device will be operating in dead battery mode and it appears the config lines are sampled only upon boot, an 8 position DIP switch (4-1825059-2 from TE Connectviity) is included to select two primary settings. The configuration involves sampling the voltage over a divider so the switch will select which resistor is used in the lower leg of the divider.

At a minimum, the VBUS should see 5V minus a small factor from the sense resistor. At 5A, the drop over the 25 mOhm resistor should be 0.125V. Thus, the VBUS should reasonably have at least 4.8V on the line at all times.

### DC-DC Output for USB PD regulation

As the voltage output from the USB PD port can be negotiated, and range from 5-20V, the system should be prepared to regulate the VBUS down to a level suitable for an LDO to feed the rest of the circuitry. This is due to the design feature that a higher input voltage may be negotiated so that other components or expansions can have access to a higher power, such as in the case where a motor is to be added to the board. This is accomplished through a DC-DC buck converter. The logic bus should not require high levels of current but does need to provide a stable output. Thus, a 3A rated buck regulator could be sufficient.

Since 3.3V is the main line, it should be stable going into the system. Since there are typically concerns with switching converters adding noise to the system, the design utilizes a LDO after the switching converter to remove noise. The chosen buck converter is the [MP2348](https://www.monolithicpower.com/en/mp2348.html?srsltid=AfmBOooL3iI7wVF1rxo_PiJ6kU1UF4-XdB7CvVGoOtTbpMCHjWyELhaH), a high efficiency simple package that can provide up to 4A with a switching frequency of 650 kHz. The datasheets shows higher efficiencies for a lower voltage inputs (e.g. 6.5V) and higher voltage outputs (e.g. 5V). The minimum input voltage is 4.2V.

TPS62933. The F version has continuous current mode in order to keep low ripple in all conditions. The O version operates out of the noise band. Max duty cycle of 98%. To achieve low frequency efficiency, base version uses CCM > DCM > PFM where frequency is adjusted

ALT: <https://www.ti.com/product/TPS62933O>

The O version is ok, the P version is just a power-good variant that uses PG to signal if the power is ready. Output voltage is set by the voltage divider and . The is set to 10kohm resistor, . Solving for the top resistor:

At 500 kHz

1.68 uH minimum for 5V input

3.6 uH minimum for 9V input

4.56 uH minimum for 15V input

4.92 uH minimum for 20V input

5.056 uH minimum for 22.8 input

5.1 uH minimum for 24V input

5.22 uH minimum for for 27.7V input

5.23 uH minimum for for 28V input

Choosing nearest value of 5.1 uH or 5.6 uH. The TVS1800 clamping diode should clamp the input voltage at 22.8V. This sets the new K value of 0.396. The maximum from the datasheet, the calculated peak current is calculated as follow:

The current is calculated from the equation:

It follows that the inductor should have a rating of 5.1 uH, have a saturation current of 10 A, and RMS current rating of 6.5A.

The recommended inductor for this design from TI’s workbench is 5.6 uH. Higher inductor values increase cost and DCR but generally reduce ripple current. Using an inductor

A similar product to the one recommend in the datasheet is 74439346056.

**78433290510**

SDR1307-5R6ML

Shielded Inductors

|  |  |  |  |
| --- | --- | --- | --- |
| Inductor P/N | Manufacturer | Cost | Description |
| SRP8540A-5R6M | Bourns | 0.53 | 5.6 uH, 30 mohm, 7.6A rms, 17A sat |
| [SRP1038AA-5R6M](https://www.mouser.com/ProductDetail/Bourns/SRP1038AA-5R6M?qs=CiayqK2gdcL4nvewsi77Ug%3D%3D) | Bourns | 0.68 | 5.6 uH, 22.8 mOhms, 8A rms, 14.1A sat |
| [SRP6060FA-5R6M](https://www.mouser.com/ProductDetail/Bourns/SRP6060FA-5R6M?qs=MLItCLRbWsxLUQxbwaGgMA%3D%3D) | Bourns | 1.64 | 5.6 uH, 15.8 mOhms, 7.5A rms, 10 sat |
| 74439346056 | Wurth Elektronik | 4.04 | 5.6 uH, 15 mOhms, 9.9A rms. 9.9A, 13.6A sat |
| [PA5432.562NLT](https://www.mouser.com/ProductDetail/Pulse-Electronics/PA5432.562NLT?qs=pUKx8fyJudACRr0COJ8pwg%3D%3D) | Pulse Electronics | 1.91 | 5.6 uH, 15.9 mOhms, 9. |
| [IHLP4040DZER5R6M01](https://www.mouser.com/ProductDetail/Vishay-Dale/IHLP4040DZER5R6M01?qs=UUKq9QDXQ0k7O9bH7nql%2Fg%3D%3D) | Vishay/Dale | 1.31 | 5.6 uH, 17.6 mOhms, 8.5A rms, 16.0A sat |

Choosing [SRP6060FA-5R6M](https://www.mouser.com/ProductDetail/Bourns/SRP6060FA-5R6M?qs=MLItCLRbWsxLUQxbwaGgMA%3D%3D) as it fits the specs and has a smaller size with low DCR for a good average price of $1.64.

100 mA seems to be the crossing point for a lot of designs from light load to more

TPS56637 – option 2,

TPS54335-2A – option 3, ok but older with higher resistance MOSFETS, [MOUSER](https://www.mouser.com/ProductDetail/Texas-Instruments/TPS54336ADDA?qs=1CfNGUMoiQ9kh21wjoJyjQ%3D%3D)

TPS62933 – option 4, good efficiency across whole range, 2021

TPS563300 – [link](https://www.ti.com/lit/ds/symlink/tps563300.pdf?ts=1733695302679&ref_url=https%253A%252F%252Fwww.ti.com%252Fproduct%252FTPS563300), good max duty cycle, decent mosfet resistance, 500 kHz fixed frequency, good efficiency, $0.87

TPS51386RJNR – $0.78, above 90% efficiency across VIN ranges, VQFN package and better thermal dissipation, new chip, V\_EN limited to 6,m Ven limited to 55.5V

A screenshot of a computer

Description automatically generated

It is noted that for 5V output, VIN should at least be 6.5V. The initial target operation is to regulate from 5V down to around 3.8V. The expected duty cycle is around 76% (3.8/5), but could be as high as 80% (3.8/4.8). The datasheet indicates there is a minimum off time of 190 ns. The period for a 650 kHz signal is 1.54 us. To adhere to the minimum off time, the max duty cycle is thus . If Vin is 4.8V, the max output can be 4.2V. If Vin is 5.0V, the output can be at max 4.38V.

The LDO chosen is the [**LD39200PU33R**](https://www.digikey.com/en/products/detail/stmicroelectronics/LD39200PU33R/5131797), which can output 2A with a maximum of 0.25V droupout and a PSSR of around 40-50 at 500 kHz. It is also a very cost effective chip at around $1/unit. While it does limit the current supply further, its cost effectiveness and other performance qualities make it the desired choice for this design. With a max 0.25V dropout, a suitable input voltage should be or greater. This provides some headroom for the LDO and some room for the buck converter to scale down. A nominal selection for the LDO is 3.6V.

There is some concern that the buck converter will be operating near or above its practical max duty cycle based on the note the note about providing a 6.5V input for a 5V output, a duty cycle of 76%. If this ratio is to be followed, the output voltage of the buck should be lowered to 3.6V at least to account for an input voltage of 4.8V. This could be the best compromise in terms of buck output and LDO input without adding components. In the case this is not sufficiency for the buck, the intermediate bus could be lowered a bit more: the LDO has a typical dropout of 135 mV, so a buck output of 3.435V could be used.

Regarding power dissipation, the buck converter at 2A output should see a dissipation of around . This dissipated power leads to a junction temperature of . If a 0.5A load is drawn by the system, the heat rise should be around 11C. This is acceptable.

#### Notes about inductor and load currents

In fixed frequency mode and in the high-side switch on time, the SW pin voltage swings up to approximately and the inductor current increases with slope . Note that this does not depend on the output current. When the high-side switch is turned off and the LS switch is turned on, the inductor current discharges through the low-side switch with a slope of . Note again that the slope does not depend on the output current. When the output current is always above 0, the mode is CCM. Thus, a larger inductor will decrease the slopes of both phases.

When the load current, e.g. 300 mA, is lower than half of the peak-to-peak inductor current in CCM, the devices enter DCM. At an even lighter load, pulse frequency modification is used to maintain high-efficiency. When either the minimum high-side on time, or the minimum peak inductor current is reached, the switching frequency decreased to maintain regulation. It is noted that the current comparator in the TPS catches the peak inductor current only, the average load current entering PFM varies with the application and external LC filters. The high-side MOSFET is turned on in bursts to provide energy to the load. When zero current crossing is detected, the low-side MOSFET is turned off. The lowest selectable frequency possible is 200 kHz. The minimum switching frequency, presumably when in light current mode, is 30 kHz.

Under high load currents near the maximum, such as 2A or 3A, the switching frequency can be increased to 1 MHz or so to accommodate the load change and higher input voltages.

Under low load currents

#### Buck regulator component configuration

Current into the enable pin should be limited to prevent excess current above 40 uA from flowing into the diode. The datasheet indicates this can be done with a pullup resistor connected to Vin. The equation given is . At maximum, the input voltage is 20V. This solves to: .

Soft start is governed by

The mode of the buck converter can be controlled by the MODE pin. These include:

1. Forced PWM
2. PFM with ultrasonic mode under light-load conditions
3. PFM mode without ultrasonic mode

The output voltage is set by a voltage divider. The datasheet gives . It also states thar a small R2 leads to considerable quiescent current loss while a large R2 makes FB noise sensitive. The recommended value for R1 is 40.2 kOhm across most ranges, including the 3.3V range. Choosing R1 to be 40.2 kOhm allows R2 to be set for an output of 3.6V. is given to be 802 mV in the datasheet.

Feedback current should be limited to less than 50 nA.

Final selection: MP2348, MP2384C, MP2384

MP2348: 90% efficiency over whole range, 95% efficiency at 5V in. 55 C/W ambient as measured on 2-layer PCB, 64x48mm. Supply voltage 4.2 to 24V. $1.75 on Mouser. 650 kHz or less at light loads. Seems to have a bit more ripple, perhaps 12-15 mV of ripple at high current.

MP2384: very low ripple of maybe 8 mV at light loads.

<https://www.mouser.com/ProductDetail/Monolithic-Power-Systems-MPS/MP9943GQ-P?qs=493kPxzlxfIUN%2FwqEBzqKg%3D%3D>

<https://www.mouser.com/ProductDetail/Monolithic-Power-Systems-MPS/MP9473GL-P?qs=eL8B9ti3n5MiWqok8H7asw%3D%3D>

<https://www.mouser.com/ProductDetail/Monolithic-Power-Systems-MPS/MP2384CGG-P?qs=GedFDFLaBXFncJRO10qr2A%3D%3D> – LOOKS GOOD, super efficienct, but faster 700 kHz frequency

<https://www.monolithicpower.com/en/documentview/productdocument/index/version/2/document_type/Datasheet/lang/en/sku/MP4423GQ-Z> -

<https://www.monolithicpower.com/en/documentview/productdocument/index/version/2/document_type/Datasheet/lang/en/sku/MP2384GG-Z> - good across whole range, above 90%, is a variant of the MP2384C. IT is said [that](https://forum.monolithicpower.com/t/mp2384-vs-mp2384c/1805?_gl=1*19uinvu*_gcl_au*MTI1Mjc1NDYwLjE3MzMzNjgyNzg.*_ga*MjAzMDI2Nzc3My4xNzMzMzY4Mjc4*_ga_XNRPF6L9DD*MTczMzU3ODg1MS40LjEuMTczMzU3ODg5OS4xMi4wLjA.&_ga=2.71038672.1779404359.1733578851-2030267773.1733368278) the C version will have a better vout ripple due to FCCM, but a worse efficiency. There is no pulse skip mode at light loads in the base version so it will have worse ripple.

**MP2395 – ok, but not as good for lower output voltages**

MP2328

MP2349

**MP2348 – looks pretty good**

[MP2315S](https://www.mouser.com/ProductDetail/Monolithic-Power-Systems-MPS/MP2315SGJ-Z?qs=Zwj7mHVHPHQK3n9ExaDQiw%3D%3D) – on Mouser for 2.29, simple package but up to 3A, good power efficiency at lower input voltages, 500 kHz switching frequency, max dissipation is 1.25W, Max duty cycle is 95% for Vfb = 750 mV

LDO Selection

[**LD39200PU33R**](https://www.digikey.com/en/products/detail/stmicroelectronics/LD39200PU33R/5131797), 2A out with 0.25V dropout at $0.99, PSSR around 44 dbs at 500 kHz

[**RP108J331D-T1-FE**](https://www.digikey.com/en/products/detail/nisshinbo-micro-devices-inc/RP108J331D-T1-FE/10215597), 3A out with 0.56V dropout at $1.36,

BUCK/BOOST

MP4245 – $6.1

MP28167-B – 4.24

MP28167-N

<https://www.monolithicpower.com/en/documentview/productdocument/index/version/2/document_type/Datasheet/lang/en/sku/MP28167GQ-A>

### 3.3V for logic and STM32

The STM32 needs a stable 3.3V reference for most peripherals. The internal SMPS can be used to feed the main and RF regulators but not the low power regulator, wakeup domain, LCD, or analog domain, or USB domain. Thus, a regulator is required to adjust the output from the USB port. A DC-DC buck boost converter is used to provide a fixed output such as 3.6-4V to the downstream. It is noted that the STM32 indicates it uses very low power to run, perhaps 20 mA or less, by looking at the Power Consumption Calculator (PCC) tool in the STM32Cube IDE.

The selected default backlight display, [C404A-FTW-LW63](https://focuslcds.com/product/c404a-ftw-lw63/), can use up to 120 mA for the backlight.

A mini speaker, such as the CMS-151103-088SP from Same Sky, is an 8 ohm speaker with input power of 0.7W. This should correspond to a current usage of

A piezo buzzer should only use maybe 5-10 mA.

An SD card could 30-100 mA.

#### Low current draw considerations

In cases where system current draw is low and the USB input is set to 5V, the utility of the DC-DC switching regulator is not as great as the case when higher voltages are input into the system. Note that efficiency for the DC-DC block becomes mostly constant starting around 0.02 mA for the base, type O, and type P models. A quick analysis in the 5V case indicates whether the design should include a mode to swap between the using VBUS directly or always going through the buck converter.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Current | LDO Power Dissipated | DC-DC Power Dissipated | LDO Temp Rise, C | DC-DC Temp Rise, C |
| 50 mA | 85 mW | 20 mW | 3.4 | 1.2 |
| 100 mA | 170 mW | 40 mW | 6.8 | 2.4 |
| 200 mA | 340 mW | 80 mW | 13.6 | 4.8 |

Section 9.3.2 of the TPS6293x datasheet indicates that there is a minimum peak inductor current, rated at . It is anticipated that most downstream circuitry will not draw nearly that much on average. It is said that when the load current is less than half of the peak-to-peak current, the device will operate in DCM.

[TPS2120](https://www.ti.com/lit/ds/symlink/tps2120.pdf?ts=1734040247940&ref_url=https%253A%252F%252Fwww.ti.com%252Fproduct%252FTPS2120)

### VBAT for RTC

When VDD is not present, VBAT operation is automatically activated. When the microcontroller is supplied only from VBAT, as it would be when USB-C is disconnected, external interrupts and RTC alarm/events do not exit it from VBAT operation. The VBAT pin should be connected to the battery. The valid voltage range is from . In section 6.3.2 of the datasheet it is recommended that VBAT fall within . Current consumption data is given for 1.8V, 2.4V, 3.0V, and 3.6V. A very common battery type is the CR2032, which is a 3V coin-cell battery. It is nominally 3.2mm thick and 20mm in diameter.

The BAT-HLD-001 from TE Connectivity provides a cost-effective and simple battery holder.

## Multiple Power Sources

The design should have at least 2 power sources, the main bus and a local battery for RTC operations. An additional battery source or input terminal, besides USB-C, can be included for convenience or evaluation.

### Local Battery

Typically batteries for battery supplies operate at 3V, the CR2023 being one example. These are typically 20mm in diameter.

[TE Con Battery Holder Link](https://www.digikey.com/en/products/detail/te-connectivity-linx/BAT-HLD-001-THM/3044009?_gl=1*10no8pn*_up*MQ..&gclid=Cj0KCQjwztOwBhD7ARIsAPDKnkAVl-omgrW-V7a-AVtoaE2QZEPQHywOrfch-0X9evkTW-sQ3L3zPZgaApR6EALw_wcB)

## Real-Time Clock

In order to have a RTC, an external battery must be included to provide VBAT.

The uC has a battery charging circuit and can be activated when VDD is present.

LSCO pin

OSC32\_OUT pin provides clock?

OSC32\_IN and \_OUT ports can supply input to the LSE clock used to generate the 1-second clock for RTC.

## Character Display

The ability to power and write to a small character display is made available by exposing the pins needed. The display chosen as a reference is the [C204A-FTW-LW63](https://focuslcds.com/product/c204a-ftw-lw63/) from FocusLCDs, which is a 20x4 character display with backlight. It uses a 3.3V input and a 4 or 8-bit interface. It is roughly 3.9 by 2.4 inches. The pinout is given in the datasheet and uses a 1 x 16 pin header for all data and power pins. The pitch given is 2.54 mm.

In 4-bit mode, only 4 lines are needed to set the character display. The pinout below is taken from the datasheet. However, data is sent in nibbles then so two transactions are required to write data or a command. The FocusLCD [website article](https://focuslcds.com/journals/break-down-of-a-parallel-interface/?srsltid=AfmBOopbbiziXuHUgvugt_7WjOh3LS8rwjkJNCKrJj8tgkYwGZSwBcBg) links the [embeddedcraft.org](http://www.embeddedcraft.org/lcd4bit.html.) tutorial on 4-bit operation. In general, it is indicated that to write two nibbles the data must be set and followed with a pulse on the enable line a total of two times.

A screenshot of a computer

Description automatically generated

The V0 pin is used to modify the contrast of the screen. The [application note](https://focuslcds.com/journals/application-notes/adjusting-the-contrast-of-an-lcd-module/) by FocusLCDs indicates that V0 should be wired to a voltage divider or potentiometer of 10k.

<https://www.mouser.com/ProductDetail/Amphenol/N6L30T3N-103-3030?qs=Rp5uXu7WBW%252B8ZM8WtY2TfQ%3D%3D>

[3362P-103LF-ND](https://www.digikey.com/en/products/detail/bourns-inc/3362P-1-103LF/1088412?gclsrc=aw.ds&&utm_adgroup=General&utm_source=google&utm_medium=cpc&utm_campaign=PMax%20Shopping_Supplier_Bourns_0118_Co-op&utm_term=&utm_content=General&utm_id=go_cmp-20514526774_adg-_ad-__dev-c_ext-_prd-1088412_sig-CjwKCAiApY-7BhBjEiwAQMrrEU76IqBgOSEPhYpK4WGT8y8cJTD9Fkq2F86J8jaD4lm-cdVP529cSRoCV1gQAvD_BwE&gad_source=1&gclid=CjwKCAiApY-7BhBjEiwAQMrrEU76IqBgOSEPhYpK4WGT8y8cJTD9Fkq2F86J8jaD4lm-cdVP529cSRoCV1gQAvD_BwE&gclsrc=aw.ds) is a good potentiometer.

A simple display able to display characters is appropriate for this design. It is expected that an RGB/parallel interface will not be native to the STM32 line so a SPI-based display is an acceptable interface.

One display that could be appropriate for the application is a character LCD display from FocusLCDs (C204AS-FTW-LW63 - [focuslcds.com](https://stg-focuslcds-staging.kinsta.cloud/product/c204as-ftw-lw63/)). This display is transreflective, meaning it should not require a backlight.

A larger, 40 x 4 chararacter display, that is also transreflective is the [C404A-FTW-LW63](https://focuslcds.com/product/c404a-ftw-lw63/) from FocusLCDs which retail for about $30. It also utilizes the parallel connection. It uses a 2x9 set of vias with standard 2.54mm pitch. The backlight typically uses 60 mA but up to 120 mA with 2-3 mA for the digital side.

Character LCD displays contain 14 pins if no backlight is attached ([focuslcds.com](https://focuslcds.com/journals/intro-to-lcd-display-programming-character-lcds/#:~:text=Character%20LCD%20displays%C2%A0contain,displays%2C%20so%20pay%20attention!)). There are 8 data pins, an enable signal, a R/W pin, register select, and 3 power pins. If necessary, 4 pins can be used instead of 8 for data lines.

## EMC/EMF Testing Ready

Without specialized tools, internal testing will be limited. The design should utilize best practices, use simulations where possible, and design in test points if they are applicable. In lieu of test results from the assembled system, a route to perform tests should be provided. This includes any tests that could possibly be down internally with the addition of an inexpensive tools and where to send the device for external tests.

## Antenna Tuning Ready

The device should support the ability to tune the antenna using data gathered from testpoints or usage. The recommended antenna to use is the inverted-F antenna, which will have a fixed design but might be able to be tuned using the matching components.

## Bootloader from Serial Memory

The design should plan to use a bootloader to flash new firmware. The firmware should ideally be located in serial memory and use CRC-32 or alternatives to verify the image.

Creating a bootloader requires creating 2 projects, one for the bootloader and one for the application. Flash memory in the uC needs to be divided between the two programs.

uC Details:

Flash is organized into 4 Kbyte pages. Each page is made of 8 rows of 512 bytes. Page 0 starts at 0x0800 0000 and spans to 0x0800 0FFF. The page number is used in the software procedure to erase a page. Page erase time is ~22 ms and max programming time for 1 Mbyte is 11 ms. The granularity in the standard mode is 8 bytes.

Flash is shared between the M4 and the M0+ core.

Program and erase operations are only possible in power range 1 ().

## Audio Output

Enabling audio output can be done in various ways with various degrees of complexity. At a most basic level, a piezo buzzer can be used with a PWM input to generate sound. A more middle-ground solution would be to utilize the STM to handle some audio processing with custom audio samples and generate the analog signal directly to an amplifier to a speaker. The most complex solution would be having an audio codec chip on board, which handles a wide array of inputs/outputs as well as settings and controls.

Adding audio to the application is a nice value add but having an audio codec is out of the scope of the project. A piezo buzzer is also very simple and can be integrated with little additional work, but also with very little configurability and poses little challenge to the designer. Thus, a solution using the STM32 chip to display short audio samples / beeps / messages seems most appropriate. While adding an audio codec to increase system flexibility would be a great feature add, it would also introduce cost as well as add lots of design/config/testing time due to the increased complexity.

The simplest implementation using the STM32WB would be to only support a mono file and single speaker. Supporting stereo would require more power, components, as well as DAC outputs, and memory to store samples. Having stereo does not add a lot of value to the design/use experience.

An example 16-bit mono track sampled at 44.1 kHz for 1 second takes up about 86 kB. Thus, a FLASH chip to store the data is required to store even short samples.

### DAC

The STM32WB does not have an onboard DAC so a DAC will have to be provided. It makes sense to use a 16 bit chip to support 16-bit audio playback, except most DACs readily available on Mouser and Digikey start around $5, an example being the [DAC8551](https://www.digikey.com/en/products/detail/texas-instruments/DAC8551IADGKR/1509340).

### Audio Amplifier

The Class-D amplifier chosen is…

Reading out the sample will need to happen over an I2C or SPI bus. The paper “[Common Inter-IC Digital Interfaces for Audio Data Transfer](https://www.analog.com/media/en/technical-documentation/technical-articles/ms-2275.pdf)” by Analog Devices states that I2S, a very popular audio IC-IC transfer protocol, uses a typical clock rate of 512 kHz for an 8 kHz signal and 12.288 MHz for a 192 kHz sample rate.

A timer will be configured to operate at the specified sampling frequency to change the DAC input.

The STM32WB supports both DMA and QSPI which can speed up reading from an external device.

Memory-mapped mode allows external flash memory to be seen by the system as if it were an internal memory.

A possible speaker to implement would be the [CMS-151103-088SP](https://www.cuidevices.com/product/resource/cms-151103-088sp.pdf). It is rated at 0.7W with 8 ohm impedance. This means the typical voltage level should be ,

The Serial Audio Interface sends data from memory (local or external) to an audio codec chip, which then drives a DAC output into an amplifier. Common bit depths include 16 bit, 24 bit.

Can use following audio protocol:

* I2S, LSB or MSB justified
* PCM/DSP
* TDM
* AC’97
* SPDIF out

### Audio Codec IC

To convert the file format to a useable input code by a DAC, an audio codec chip can be used. The chip handles interpreting the file format and standardizing the output to digital codes for the DAC. To have stereo sound, two channels must be output to a DAC(s) and amplifiers.

|  |  |  |  |
| --- | --- | --- | --- |
| **Device** | **Manufacturer** | **Price** | **Description** |
| [SGTL5000XNLA3](https://www.mouser.com/ProductDetail/NXP-Semiconductors/SGTL5000XNLA3?qs=sGAEpiMZZMuGeGLVV4AlaXDPLJJLEwgRW5gQ9lWdOP0%3D) | NXP Semiconductors | 3.66 | 24 bit, 96 kHz, I2C / SPI, 1.62 to 3.6V, 1 channel |
| [6PAIC3109TRHBRQ1](https://www.mouser.com/ProductDetail/Texas-Instruments/6PAIC3109TRHBRQ1?qs=sGAEpiMZZMuGeGLVV4Alaei%2FfOAnaxFBlBkUBMqGygE1TN2pwhvlNw%3D%3D) | Texas Instruments | 3.52 | 16 bit, 96 kHz, I2C, 1.8 / 3.3V, mono, 1 channel |
| [TLV320AIC3101IRHBR](https://www.mouser.com/ProductDetail/Texas-Instruments/TLV320AIC3101IRHBR?qs=sGAEpiMZZMuGeGLVV4AlaUH1mFnnbOAhadf13BMDy2U%3D) | Texas Instruments | 3.00 | Multiple bit rate, stereo 8 ohm 0.5W speakers supported, |

[TLV320DAC3203IRGER](https://www.mouser.com/ProductDetail/Texas-Instruments/TLV320DAC3203IRGER?qs=sGAEpiMZZMuGeGLVV4AlaY1ReVQJEZKAR%2F152BtTwt8%3D)

[TLV320AIC3101IRHBR](https://www.mouser.com/ProductDetail/Texas-Instruments/TLV320AIC3101IRHBR?qs=sGAEpiMZZMuGeGLVV4AlaUH1mFnnbOAhadf13BMDy2U%3D) – 8 ohm, 0.5W output

[**TLV320AIC3100IRHBR**](https://www.digikey.com/en/products/detail/texas-instruments/TLV320AIC3100IRHBR/2193085), has beep generator, can power a 4 ohm differential load

A note on audio outputs: there are sometimes any configuration of three outputs in audio chains. These include:

1. Speaker output, such as Class-D
2. Headphone output
3. Lineout

A lineout is typically being fed to a driven load, meaning it does not have to source as much current as a channel would for a headphone. Headphones are driven directly from the output, so the output impedance should be low and source ample current. The speaker output drives a speaker directly, sourcing the current needed while using the analog voltage from a DAC to construct the source signal.

To avoid audible hiss from amplifier noise floor, SNR in a class-D amp should exceed 90 dB in low-power amplifiers ([Analog Devices source](https://www.analog.com/en/resources/analog-dialogue/articles/class-d-audio-amplifiers.html#:~:text=Signal%2Dto%2Dnoise,satisfactory%20overall%20SNR.)).

Can any speaker use differential or single ended?

[**TAC5142**](https://www.ti.com/product/TAC5142)

## Piezo Buzzer or Speaker

PWM can be used to generate a square wave, which is then run through a LPF to round the corners.

[CEP-2224](https://www.cuidevices.com/product/resource/cep-2224.pdf), 3-20 VDC, internal drive – NO, for 12V

[AI-3035-TWT-3V-R](https://www.digikey.com/en/products/detail/pui-audio-inc/AI-3035-TWT-3V-R/1745457), 2-5 VDC, internal drive

[PS1240P02BT](https://www.digikey.com/en/products/detail/tdk-corporation/PS1240P02BT/935924), 0-30 V, external drive, zero-peak signal

## USB

The STM32WB series offers a full-speed (FS) USB 2.0 interface, 12 Mbit/s. Up to 16 endpoints are supported.

The connector appropriate for the design is a USB 2.0 connector, which does not route the additional USB 3.0 pins. This reduces pin count and soldering complexity. The primary pins that are routed are the standard D+, D-, CC1, and CC2 pins. The SBU pins, the sideband channels, that are available through the connector should be left floating as they are not used.

## Current Monitoring

The board supports current monitoring on a few power lines using a sense resistor and connected ADC. The points monitored include:

1. System monitoring through VBUS sensing
2. **Placeholder**

#### VBUS Monitoring ✅

The accuracy of the current sensing comes down to maximizing the sense resistance while limiting the power dissipation in the resistor and offset error and reduced common-mode rejection due to bias currents. A recommendation from Texas Instruments for their INAx180 line is to keep sense resistors no larger than a few ohms.

Power dissipation is governed by . 5A is the maximum allowed over USB-C lines. While I expect working to be much less, entirely bounded by the more standard 3A limit, I want to design the sense circuit to have some overhead. I will somewhat arbitrarily choose a max current of 6.3A. Damage to the circuitry will probably occur if this current is actually drawn but since it is governed by USB PD it shouldn’t be allowed anyways. A minimum current could be estimated to be 50 mA, for the purpose of the following calculations.

A good option for the current sense amp is Texas Instruments’ INAx180 series, which supports both high side and low side sensing. In this case, we are using high side sensing since the resistor is placed directly after the USB port and sees the VBUS voltage. The INAx180 has options for gains of 20, 50, 100, and 200 V/V and common mode voltages up to 26V. It does support a shutdown mode by removing the power to the power pin, though this isn’t required.

If we suppose that the max current through the resistor is 6.3A then the relationship becomes . If a 1W resistor is used, then . Thus, the initial choice is 25 mOhm.

An additional requirement is to make sure that the output voltage does not swing past the allowed rails by verifying the gain selection. The TI datasheet provides the following guidelines to verify the selection. and are given in the equations and refer to the positive and negative swing values and are provided in the datasheet in section 7.5.

If a gain of 20 is chosen, the relationships are satisfied.

At 1A drawn, power dissipation should be .

If 5A is drawn, the voltage seen over the resistor should be , which then gets amplified to A final output voltage to the system of 4.875V should be acceptable since it will get stepped down to 3.3V later anyway.

[ERJ-8CWFR025V](https://www.digikey.com/en/products/detail/panasonic-electronic-components/ERJ-8CWFR025V/4927007) is a good option for the sense resistor that is 25 mOhm with a power rating of 1W in a large 1206 package.

[INA180A1IDBVR](https://www.digikey.com/en/products/detail/texas-instruments/INA180A1IDBVR/8132986) is the appropriate model to have a gain of 20 in an SOT-23-5 package. It supports a power supply voltage of 2.7 – 5.5V to power the device. The datasheet also indicates that the device can be powered down using a logic gate or switch to drive the VS pin. Current leakage when the device is off but common mode voltage is present is said to be dictated by the bus voltage and 500 kOhm impedance in the device to ground. Small leakage should be acceptable for the short amount of time the device is unpowered.

## Configuration Details